High Accuracy Magnetic Angle Sensor IC

1. Features

- AEC-Q100 Grade0 qualified
- ISO26262 ASILB qualified
- High-Accuracy rotary absolute angle position detection
- Simple magnetic circuit design
- -40℃ to 160℃ operating temperature range
- Output modes: Analog, PWM, SPI
- Programmable angular measuring range (angles up to 360 degrees)
- Programmable linear transmission characteristics (any 4-points, 8-points, or range-selectable 16-segments, 32-segments equally divide curves)
- 32-bit programmable user ID
- Differential Hall sensing to resist stray magnetic field interference
- Disconnect diagnostics (broken V_{DD}, broken V_{SS})
- Over-current and over-voltage protection; under-voltage detection
- Package：SOP8，eTSSOP-16L

2. Product Applications

- Non-contact absolute angular position detection
- Accelerator pedal sensor
- Steering wheel angle sensor
- Shifter gear position detection
- Throttle and exhaust gas recirculation valve
- Ride height of vehicle
- Rotary switch

3. Description

The SC69401 is an angular position sensor chip based on the principle of differential Hall magnetic sensing from Semiment Electronics. A full differential Hall sensing matrix is built into the center of the chip, which generates a corresponding sine-cosine position signal by sensing a pair of polar S/N magnets above it. The signal is amplified by a preamplifier and then sampled by the internal analog-to-digital converter circuitry. The chip's proprietary DSP circuitry performs angular arithmetic, and finally outputs the absolute position information (0-360 degrees) of the magnet's rotation in a variety of interface formats.

The SC69401 provides a variety of output methods: analog output proportional to the rotation angle, PWM output, and 4-wire SPI bus. The output curve can be selected from any 4-points, 8-points, or 16-segments, 32-segments, or any other programming method.

The SC69401, a sensor chip primarily for automotive applications, provides a rich set of on-chip diagnostic functions. The chip was designed and developed following the ISO26262 standard and is ASIL-B Level.

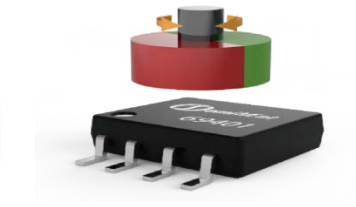

Fig.1 Installation diagram

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4. Terminal Configuration

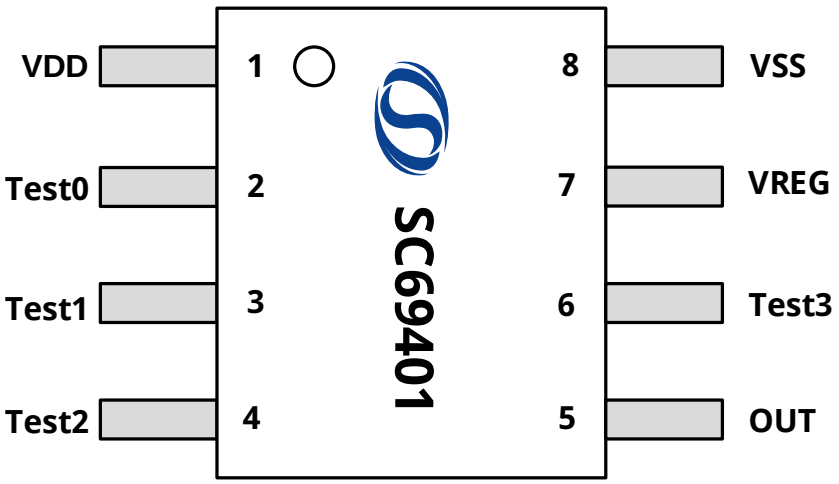


Fig.2 SOP8 Pin Description

Terminal		Type	Description
Name	Number		
VDD	1	Power	Power Input
Test0	2	Test/Digital Output	Test pin, connect to Ground; SPI_MISO: Master in Slave out data pin for SPI
Test1	3	Test	Test Pins, connect to ground
Test2	4	Test/Digital Input	Test pin, connect to ground; SPI_SCLK: SPI clock signal input.
OUT	5	Output/Digital Input	Analog output; PWM; SPI_CS: SPI enable input pin
Test3	6	Test/Digital Input	Test pin, connect to ground; SPI_MOSI: SPI master-out slave-in data pin
VREG	7	Power output	Internal power supply
VSS	8	Ground	Ground

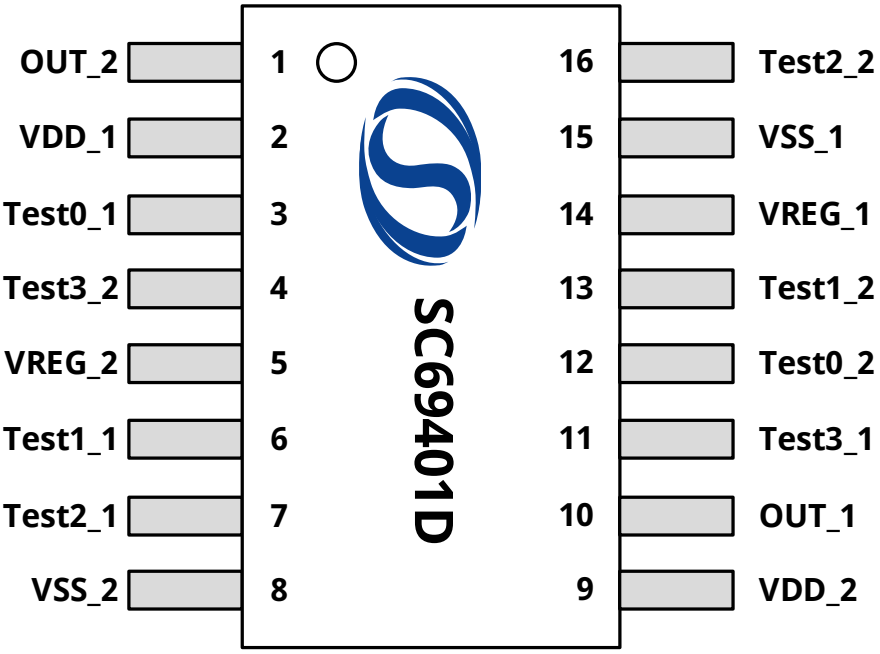


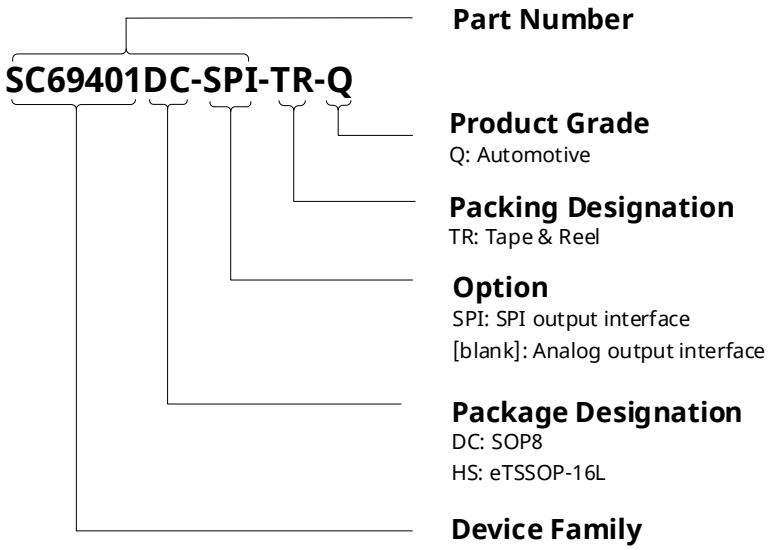
Fig.3 eTSSOP-16L Pin Description

Terminal		Type	Description
Name	Number		
OUT_2	1	Output/Digital Input	Chip 2 - analog output; PWM; SPI_CS: SPI enable input pin
VDD_1	2	Power	Chip 1 - Power Input
Test0_0	3	Test/Digital Output	Chip 1 - test pin, connect to ground; SPI_MISO: master-in slave-out data pin for SPI
Test3_2	4	Test/Digital Input	Chip 2 - test pin, connect to ground; SPI_MOSI: master-out slave-in data pin for SPI
VREG_2	5	Power output	Chip 2 - Internal Power Supply
Test1_1	6	Test	Chip 1 - test pin, connect to ground
Test2_1	7	Test/Digital Input	Chip 1 - test pin, connect to ground; SPI_SCLK: SPI clock signal input
VSS_2	8	Ground	Chip 2 - Ground
VDD_2	9	Power	Chip 2 - Power Input
OUT_1	10	Output/Digital Input	Chip 1 - analog output; PWM; SPI_CS: SPI enable input pin
Test3_1	11	Test/Digital Input	Test pin, connect to ground; SPI_MOSI: SPI master-out slave-in data pin
Test0_2	12	Test/Digital Output	Chip 2 - test pin, connect to ground; SPI_MISO: master-in slave-out data pin for SPI
Test1_2	13	Test	Chip 2 - test pin, connect to ground
VREG_1	14	Power output	Chip 1 - Internal Power Supply
VSS_1	15	Ground	Chip 1 - Ground
Test2_2	16	Test/Digital Input	Chip 2 - test pin, connect to ground; SPI_SCLK: SPI clock signal input

5. Ordering Information

Ordering Information	Marking	Option	Class	Ambient, T_A(℃)	Package	Packing	Quantity
SC69401DC-TR-Q	69401	-	Q	-40 ~ 160	SOP8	Tape & reel	4000/reel
SC69401DC-TR	69401	-	-	-40 ~ 160	SOP8	Tape & reel	4000/reel
SC69401DC-SPI-TR-Q	69401	SPI	Q	-40 ~ 160	SOP8	Tape & reel	4000/reel
SC69401HS-TR-Q	69401	-	Q	-40 ~ 160	eTSSOP-16L	Tape & reel	3000/reel
SC69401HS-TR	69401	-	-	-40 ~ 160	eTSSOP-16L	Tape & reel	3000/reel
SC69401HS-SPI-TR-Q	69401	SPI	Q	-40 ~ 160	eTSSOP-16L	Tape & reel	3000/reel

Ordering Information Format



6. Absolute Maximum Ratings

over operating free-air temperature range

Symbol	Parameter	Test conditions	Min.	Max.	Units
V_{DDR}	Power supply reverse Voltage	t＜60S	-14	28	V
V_{DD}	Output voltage	t＜60S	-6	18	V
I_R	Ooutput Reverse current		-	40	mA
T_A	Operating ambient temperature		-40	160	℃
T_{STG}	Storage Temperature		-40	160	℃
H	Magnetic Field Strength		-1	1	T

Note：
Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7. ESD Protection

Symbol	Parameter	Test conditions	Min.	Max.	Units
V_{ESD_HBM}	HBM	Refer to AEC-Q100-002E HBM standard, R=1.5kΩ, C=100pF	-4	+4	KV
V_{ESD_CDM}	CDM	Refer to AEC-Q100-011C CDM standard	-750	750	V

8. Operating Characteristics

Electrical Parameter

over operating free-air temperature range (V_{DD}=12V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage_5V	5V mode	4.5	5.0	5.5	V
$V_{DD\_3.3V}$	Supply Voltage_3.3V	V_{REG} and V_{DD} are connected to 3.3V UVLO_3P5EN=1	3.15	3.3	3.6	V
I_{DD}	Supply Current	Single die SOP8	-	8	10	mA
Isurge	Isurge Current	Single die SOP8	-	-	50	mA
I_{OCP}	Overcurrent Alarm	Single die SOP8	-	25	35	mA
V_{REG}	Regulated Voltage		3.1	3.37	3.5	V
V_{REGOVP}	Regulated Voltage Overdrive Detection		3.65	3.75	3.85	V
V_{REGUVL}	Regulated Voltage Low Detection		2.7	2.8	2.9	V
V_{UVLO}	Undervoltage Detection Voltage	UVLO_3P5EN = 0	3.4	3.7	4.2	V
		UVLO_3P5EN = 1	2.6	2.8	3.1	V
$V_{UVLOHYS}$	Undervoltage Detection Hysteresis		50	-	350	mV
V_{OVP}	Overvoltage Protection Voltage		5.8	6.2	6.6	V
$V_{OVPHYST}$	Overvoltage Detection Hysteresis		100	-	600	mV
I_{short}	Output Short-circuit Current	Shorted to V_{SS}, Analog Output	-	-	15	mA
		Short to V_{SS}, PWM Push-Pull Outputs	-	-	50	mA
		Shorted to V_{DD} Analog Output	-	-	15	mA
		Shorted to V_{DD}, PWM Push-Pull Outputs	-	-	50	mA
R_L	Analog Output Load Resistance	Pull-up resistor, connected to V_{DD}	4.7	-	470	KΩ
		Pull-down resistor, connected to V_{SS}	4.7	-	470	KΩ
R_{L_PWM}	PWM Output Load Resistance	Pull-up resistor, connected to V_{DD}	1	-	-	KΩ
		Pull-down resistor, connected to V_{SS}	1	-	-	KΩ
Vsat_lo	Analog Output Saturation Level	Pull-up resistor R=10k, connected to V_{DD}	-	0.5	2	%V_{DD}
		Pull-up resistor R=4.7k, connected to V_{DD}	-	2.5	3	%V_{DD}
Vsat_hi		Pull-down resistor R=4.7k, connected to V_{SS}	96.5	97.5	-	%V_{DD}
		Pull-down resistor R=10k, connected to V_{SS}	97.5	98	-	%V_{DD}
Dsat_lo	Active Diagnostic Output Level	Pull-down resistor R≥4.7k	-	0.5	1	%V_{DD}
		Pull-up resistor R≥4.7k	-	3.5	4	%V_{DD}

Electrical Parameter(continue)

$BV_{SS}PD$	Passive Diagnostic Output Level (broken)	Broken V_{SS}, pull-down resistor, 4.7K≤R≤47k	-	0	3	$\%V_{DD}$
$BV_{SS}PU$		Broken V_{SS}, pull-up resistor, 4.7K≤R≤47k	97	98	-	$\%V_{DD}$
$BV_{DD}PD$		Broken V_{DD}, pull-down resistor, 4.7K≤R≤47k	-	0	1	$\%V_{DD}$
$BV_{DD}PU$		Broken V_{DD}, pull-up resistor, 4.7K≤R≤47k	96.5	98	-	$\%V_{DD}$
Clamp_lo	Programmable Clamp Voltage (1)	Programmable	0	-	100	$\%V_{DD}$
Clamp_hi		Programmable	0	-	100	$\%V_{DD}$

Note :
(1) The SC69401 can meet the typical application output range shown in Figure 4

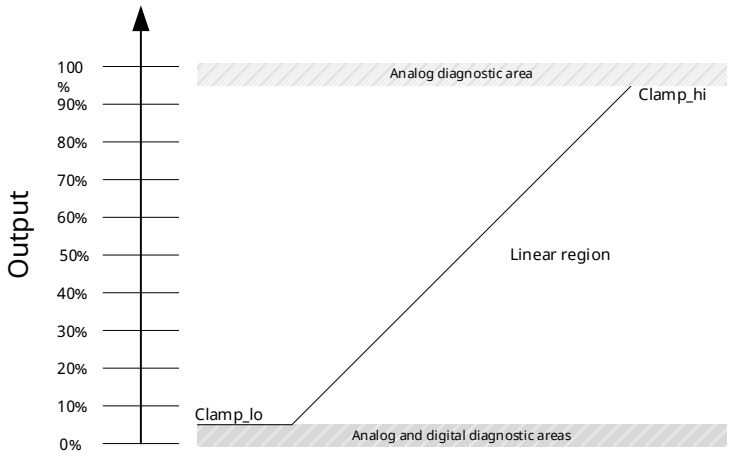


Fig.4 Typical application output range

Timing Parameter-Basic Timing

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
F_{CK}	Main Clock Frequency	Full Temperature Test	7.8	8.2	8.5	MHz
$\Delta F_{CK,T}$	Main Clock Frequency Temperature Offset		-3	-	3	$\%F_{CK}$
Tper	Data Refresh Frequency		121	128	134	us
Ts	Step Response Time		-	128	-	us
T_{POR}	Power-on Reset		-	40	-	us
T_{INIT}	Initialization Time		-	16.384	-	ms
SR	Analog Output Slew- rate	C_{OUT}=100nF	-	60	-	V/ms
		C_{OUT}=10nF	-	80	-	V/ms
		C_{OUT}=47nF	-	85	-	V/ms
		C_{OUT}=330nF	-	20	-	V/ms

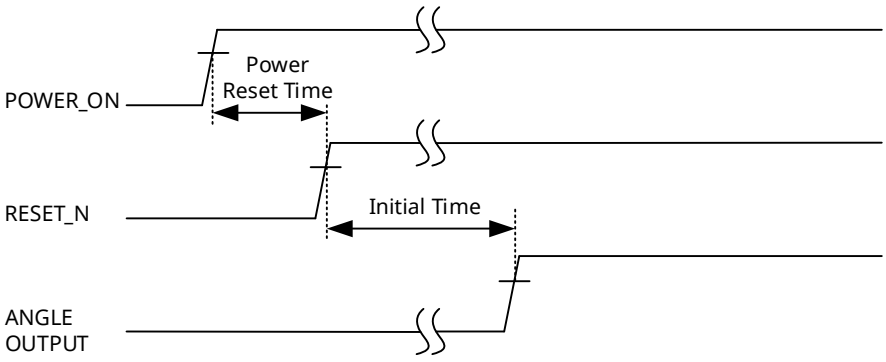


Fig.5 Power-on reset timing

Timing Parameter-EEPROM Timing

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{PS}	Power-on Reset Time		-	100	-	us
t_{PS}			-	100	-	us
TIDLE	Standby Time		-	20	-	ms

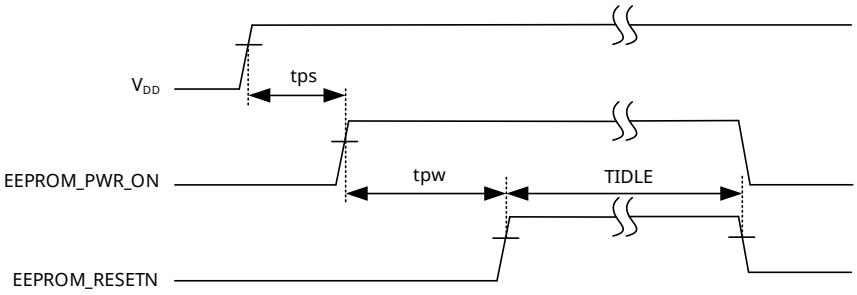


Fig.6 EEPROM timing

Timing Parameter-PWM Output

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
F_{PWM}	PWM Frequency	Frequency range	125,250,500,1000,2000			Hz
F_{PWM_Init}	PWM Frequency Initial Tolerances	25℃	-	-	±2%	F_{PWM}
ΔF_{PWM}	PWM Frequency Thermal Drift	PWM frequency temperature drift	-	-	±3%	F_{PWM}
Trise_LSD	PWM Output Rise Time (open-drain output)	4.7nF，R_L=1KΩ pull-up	-	10	-	us
		4.7nF，R_L=10KΩ pull-up	-	100	-	us
		10nF，R_L=1KΩ pull-up	-	20	-	us
Trise_PP	PWM Output Rise Time (push-pull)	4.7nF，R_L=1KΩ pull-up	-	3	-	us
		4.7nF，R_L=10KΩ pull-up	-	3	-	us
		10nF，R_L=1KΩ pull-up	-	4	-	us

Timing Parameter-PWM Output(continue)

Tfall_LSD	PWM Output Fall Time (open-drain output)	4.7nF，R_L=1KΩ pull-up	-	2	-	us
		4.7nF，R_L=10KΩ pull-up	-	2	-	us
		10nF，R_L=1KΩ pull-up	-	4	-	us
Tfall_PP	PWM Output Fall Tme (push-pull output)	4.7nF，R_L=1KΩ pull-up	-	2	-	us
		4.7nF，R_L=10KΩ pull-up	-	2	-	us
		10nF，R_L=1KΩ pull-ups	-	4	-	us

Timing Parameter-SPI Output

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		0.7*V_{DD}	-	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	-	0.3*V_{DD}	V
V_{IH}	High Level Output Voltage		V_{DD}-0.35	--	V_{DD}	V
V_{IL}	Low Level Output Voltage		0		V_{SS}+0.35	V
t_{SCLK}	Clock Cycle	EE_PINFILTER = 1	450	500	-	ns
		EE_PINFILTER = 2	900	1000	-	ns
		EE_PINFILTER = 3	1800	2000	-	ns
t_{SCLK_LO}	Clock Low	EE_PINFILTER = 1	225	-	-	ns
		EE_PINFILTER = 2	450	-	-	ns
		EE_PINFILTER = 3	900	-	-	ns
t_{SCLK_HI}	Clock High	EE_PINFILTER = 1	225	-	-	ns
		EE_PINFILTER = 2	450	-	-	ns
		EE_PINFILTER = 3	900	-	-	ns
t_{MISO}	Output Data Delay Time	EE_PINFILTER = 1, C_L = 30pF	-	-	210	ns
		EE_PINFILTER = 2, C_L = 30pF	-	-	300	ns
		EE_PINFILTER =3, C_L = 30pF	-	-	510	ns
t_{MOSI}	Data Capture Establishment Time		-	30	-	ns
t_1	Initial Clock Delay Time	EE_PINFILTER = 1	225	-	-	ns
		EE_PINFILTER = 2	450	-	-	ns
		EE_PINFILTER = 3	900	-	-	ns

Timing Parameter-SPI Output(continue)

t_2	Initial Output Data Setup Time	EE_PINFILTER = 1	-	90	120	ns
		EE_PINFILTER = 2	-	180	210	ns
		EE_PINFILTER = 3	-	370	420	ns
t_3	Communication Completion Enable Hold Time		225	-	-	ns
t_4	Communication Completion Output Hold Time	EE_PINFILTER = 1	-	90	120	ns
		EE_PINFILTER = 2	-	180	210	ns
		EE_PINFILTER = 3	-	370	420	ns
$t_{SyncPulse}$	Synchronized Pulse Period	EE_PINFILTER = 1	520	-	10000	ns
		EE_PINFILTER = 2	610	-	10000	ns
		EE_PINFILTER = 3	820	-	10000	ns

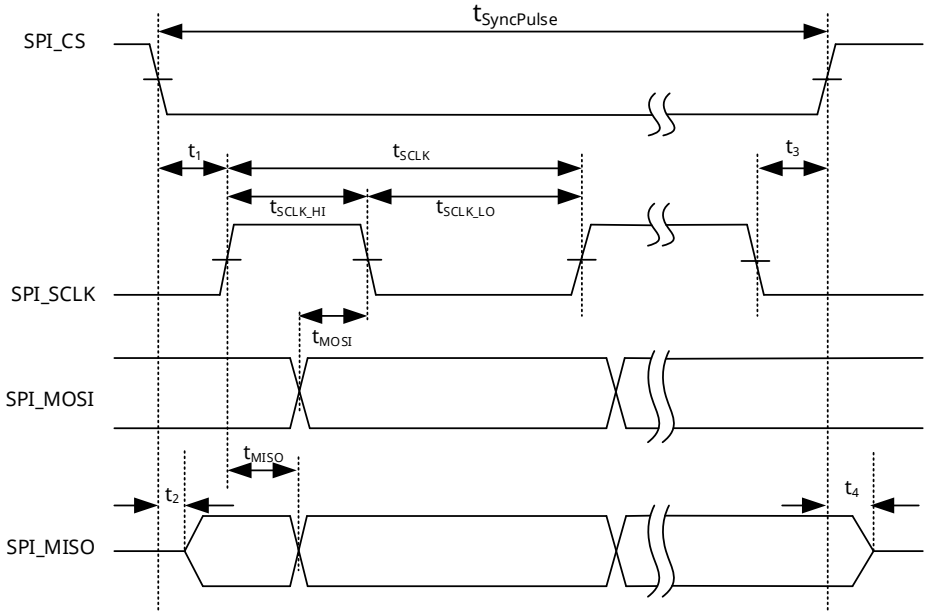


Fig.7 SPI timing

Accuracy Parameter-Analog Output

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
R_{ADC}	ADC Resolution		-	15	-	bits
R_{DAC}	Analog Output Resolution		-	12	-	bits
INL	DAC Intrinsic Nonlinearity Error		-	5	-	LSB
DNL	DAC Differential Nonlinear Error		0.05	1	3	LSB
ΔEang	Angular Offset Error		-1.2	-	1.2	Deg
ΔE_L	Nonlinearity Error		-1	-	1	Deg
ΔEtemp	Angular Temperature Drift Error		-0.5	-	0.5	Deg
ΔEratio	Proportional Output Error	$4.5V \le V_{DD} \le 5.5V$	-0.05	0	0.5	$\%V_{DD}$
N_{pk-pk}	Output Pole Noise		-	0.18	0.27	Deg

Accuracy Parameter-PWM Output

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
RSP	PWM output resolution		-	12	-	bits
J_{DC}	PWM % Duty Cycle Jitter (open-drain output)	125Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up	-	±0.003	±0.016	%DC
		250Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up	-	±0.005	±0.02	%DC
		500Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up	-	±0.009	±0.035	%DC
		1000Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up	-	±0.003	±0.016	%DC
		2000Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up	-	±0.005	±0.02	%DC
J_{DC}	PWM % Duty Cycle Jitter (push-pull output)	125Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up	-	±0.003	±0.016	%DC
		250Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up	-	±0.005	±0.02	%DC
		500Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up	-	±0.009	±0.035	%DC
		1000Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up	-	±0.003	±0.016	%DC
		2000Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up	-	±0.005	±0.02	%DC
J_{PWM}	PWM Frequency Jitter (open-drain output)	125Hz-2000Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up		±0.04	±0.15	Hz
J_{PWM}	PWM Frequency Jitter (push-pull output)	125Hz-2000Hz,4.7nF,R_L=1Kohm, Resistor Pull-Up		±0.04	±0.15	Hz

Magnetic Parameter

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
H_{EXT}	Magnetic Field Strength		10	-	120	mT
D_{mag}	Magnet Diameter		-	6	-	mm
H_{mag}	Magnet thickness		-	2.5	-	mm
AG	Airgap of Magnet and Chip		0.5	-	3	mm
	Magnet Material		-	NdFeB 35	-	-

9. Block Diagram

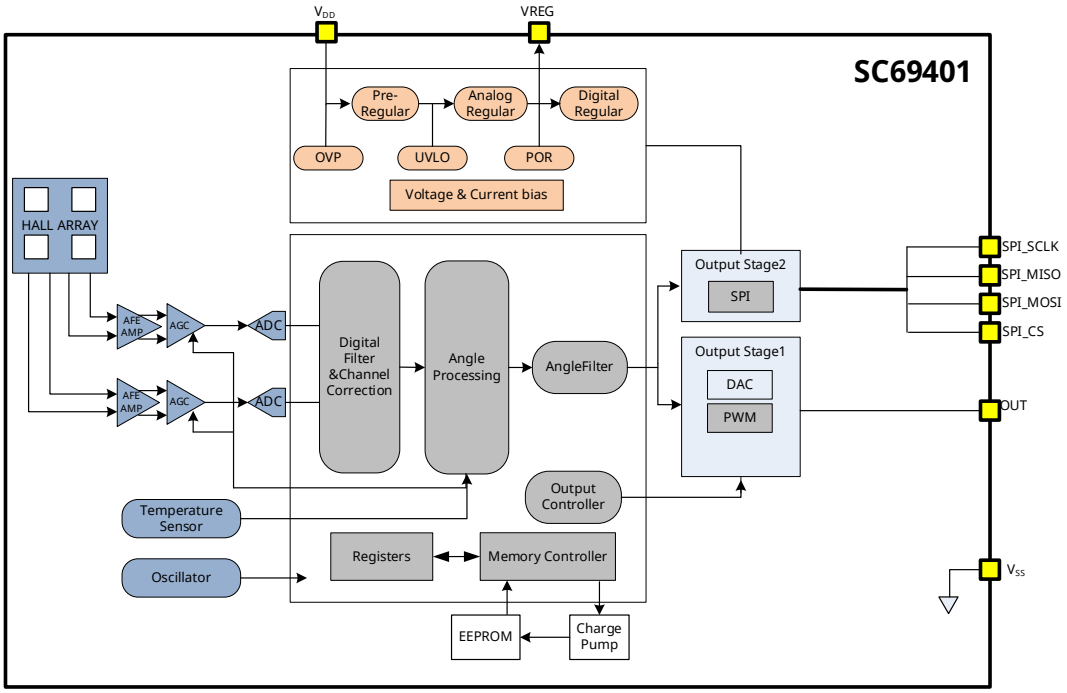


Fig.8 Block Diagram

10. Function Description

User Programmable Parameters

Parameter	Description	Default	Bit
OUT mode	output mode	0	2
PWM POL	PWM Polarity	0	1
PWMT	PWM frequency	0	3
OUT_CONFIG	PWM Output Configuration	0	2
GAIN_G	Analog op amp first stage gain setting	0	2
AGC	Automatic gain control of the second stage of an analog op amp	1	1
GAIN_F	Analog op amp second stage gain setting	1	5
SEMI_ID1	Semiment Factory ID	xxx	8
SEMI_ID2	Semiment Factory ID	xxx	8
SEMI _ID3	Semiment Factory ID	xxx	8
SEMI _ID4	Semiment Factory ID	xxx	8
USER_ID1	User ID	0	8
USER_ID2	User ID	0	8
USER_ID3	User ID	0	8
USER_ID4	User ID	0	8

EEPROM_LOCK_CODE	EEPROM_LOCK Bit Valid Judgment Code	0	7
EEPROM_LOCK	EEPROM Lock Bit	0	1
DIAG_EN	Diagnostic Enable Bit	1	1
DIAG_MASK	Diagnostic Mask Register	128	8
GAIN_THRESHOLD_LOW	Analog op amp second stage gain low thresholds	0	5
GAIN_THRESHOLD_HIGH	Analog op amp second stage gain high thresholds	31	5
FIELDTHOLD_LOW	Low field strength threshold	0	8
FIELDTHOLD_HIGH	High field strength threshold	255	8
TEMPTHRESHOLD_LOW	Low temperature threshold	0	7
TEMPTHRESHOLD_HIGH	High temperature threshold	127	7
DIAG_DEBOUNCE	Diagnostic debounce time	0	3
CLAMP_HIGH	Output High Clamp	65535	16
CLAMP_LOW	Output Low Clamp	0	16
DP	Break point/Zero Point	0	16
CW	Direction of rotation	0	1
WORK_RANGE_GAIN	16-point/32-point calibrated operating angle range (degrees)	360	16
LNR_POINTS	Calibration point selection	3	2
LNR_A_X	4-point calibration , X-axis coordinates (angle)	0	16
LNR_B_X		0	16
LNR_C_X		0	16
LNR_D_X		0	16
LNR_A_Y	4-point calibration , Y-axis coordinates (%V_{DD})	0	16
LNR_B_Y		0	16
LNR_C_Y		0	16
LNR_D_Y		0	16
LNR_A_S	4-point calibration, slope of each segment	0	16
LNR_B_S		0	16
LNR_C_S		0	16
LNR_D_S		0	16
LNR4_S0	4-point calibration, initial slope	0	16
LNR4_Y5	4-point calibration, endpoint Y coordinate	0	16
LNR_Y0	4-point, 16-point/32-point calibration of the initial point Y-coordinate	0	16
LNR9_Yn	8-point calibration, Y-axis coordinates (n=0~8)	0	9x16
LNR9_Xn	8-point calibration, X-axis coordinates (n=0~8)	0	9x16
LNR17_Yn	16-point calibration, Y-axis coordinates (n=0~15)	0	17x16

LNR_DELTAYn	32-point calibration, Y-axis coordinates (offset %) (n=0~31)	0	32x8
LNR_DELTA_Y_EXPAND	32-point calibration, Y-axis coordinate deviation range setting	3	2

Output Mode

The SC69401 provides three output modes: proportional analog output, PWM output, and SPI bus output. PWM supports PMOS or NMOS open drain output and push-pull output, SPI only supports push-pull output.

Analog Output Mode

Parameter	Value	Description
OUT mode【1:0】	0	analog output
	1	PWM output
	2	reserve
	3	SPI output

PWM Output Mode-Polarity setting

Parameter	Value	Description
PWM POL	0	Active High
	1	Active Low

PWM Output Mode-Frequency setting

Parameter	Value	Description
PWMMT【2:0】	000	125
	001	250
	010	500
	011	1000
	others	2000

PWM Output Mode-Output Mode Setting

Parameter	Value	Description
OUT_CONFIG【2:0】	0	Digital Output NMOS Open-Drain
	1	Digital Output PMOS Open-Drain
	2	Digital Push-Pull Output
	3	Digital High Resistance State Output

PWM Output Mode -Output Wave

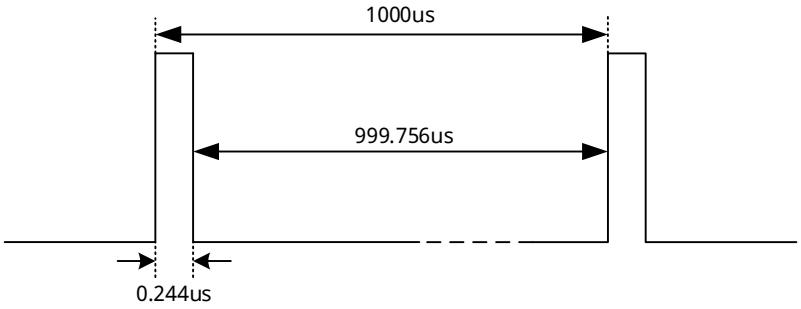


Fig.9 PWM Output Wave when PWM_POL=0

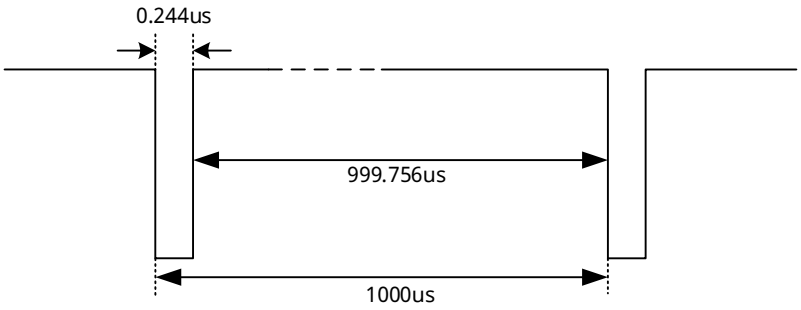


Fig.10 PWM Output Wave when PWM_POL=1

4-Wire SPI Protocol Output

SC69401 SPI is used as a full-duplex serial communication, in which the host can send commands and receive the result of the last command at the same time in one master-slave communication.SC69401 is used as a slave and controlled by the chip select signal SPI_CS.SPI communication is activated when SPI_CS is set to low level, and ends when SPI_CS is set to high level. SPI_SCLK is used as a clock for SPI communication, which is sent by the host to SC69401.MISO and MOSI signals are changed on the rising edge of the clock and captured on the falling edge of the clock.

Command	Transmission Direction	Byte 0	Byte 1	Byte 2	Byte 3
Reads 16-bit angle values	Master to Slave	0x9C	0x00	0x00	CRC8
	Slave to Master	0x9C	AngleH	AngleL	CRC8
Read temperature and magnetic field strength values	Master to Slave	0xBC	0x00	0x00	CRC8
	Slave to Master	0xBC	Temp	FiledStrength	CRC8
Write Register Value	Master to Slave	0xCC	RegAddr	RegValue	CRC8
	Slave to Master	0xCC	RegAddr	RegValue	CRC8
Read Register Value	Master to Slave	0xC4	RegAddr	0x00	CRC8
	Slave to Master	0XC4	RegValue	(RegAddr+1) Value	CRC8

Sensor Front-End Setup

First stage gain setting

Parameter	Value	Description
GAIN_G【2:0】	0	2.5
	1	5
	2	10
	3	10

Second stage gain setting

Parameter	Value	Description
AGC	0	Disable automatic gain control
	1	Enable automatic gain control
GAIN_F【4:0】	0	1
	1	1.1
	2	1.21
	...	...
	29	15.86
	30	17.4
	31	20

Traceablility Information

At the factory, each device contains the Semiment factory ID and user ID for traceable purposes.

Parameter	Value
SEMI_ID1【7:0】	0-255
SEMI_ID2【7:0】	0-255
SEMI_ID3【7:0】	0-255
SEMI_ID4【7:0】	0-255
USER_ID1【7:0】	0-255
USER_ID2【7:0】	0-255
USER_ID3【7:0】	0-255
USER_ID4【7:0】	0-255

EEPROM Write Protection

Parameter	Value	Description
EEPROM_LOCK_ CODE【6:0】	0x3A	EEPROM_LOCK bit active
	others	EEPROM_LOCK bit inactive
EEPROM_LOCK	0	EEPROM can be read，written and erased
	1	EEPROM read-only

Diagnostic

Diagnostic Enable

Parameter	Value	Description
DIAG_EN	0	Enable Diagnostics
	1	Disable Diagnostics

Diagnostic Mask Register

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CRC Checksum Error	GAINF overflow	Current diagnosis	Digital Voltage Fault	CORDIC overflow	Field strength overflow	ADC overflow	Temperature overflow

Diagnostic Threshold

Parameter	Value	Description
GAIN_THRESHOLD_LOW【4:0】	0-31	Second-stage analog op-amp gain low thresholds
GAIN_THRESHOLD_HIGH【4:0】	0-31	Second-stage analog op-amp gain high thresholds
TEMPTHRESHOLD_LOW【6:0】	0-127	Low-temperature threshold
TEMPTHRESHOLD_HIGH【6:0】	0-127	High-temperature threshold
FIELDTHOLD_LOW【7:0】	0-255	low field strength threshold
FIELDTHOLD_HIGH【7:0】	0-255	High field strength threshold

Diagnostic Debounce Time Setting

Parameter	Value	STEP_UP TIME(ms)	STEP_DOWN TIME(ms)
DIAG_DEBOUNCE【2:0】	0	20	20
	1	20	30
	2	20	40
	3	40	40
	4	60	80
	5	80	100
	6	100	120
	7	120	140

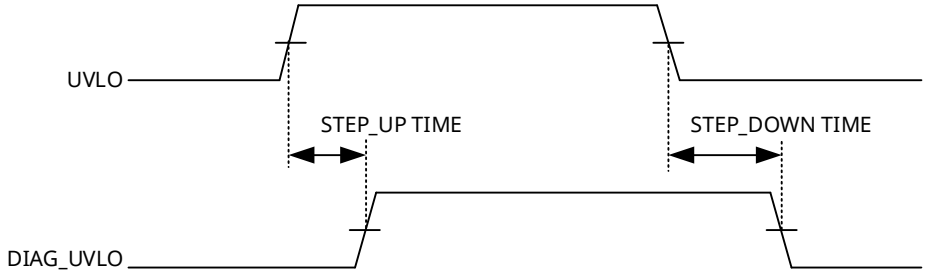


Fig.11 Diagnostic Debounce Timing

Output Parameter Setting

Breakpoint/Zero-DP

The breakpoint and zero point of the SC69401 are the same point, which can be programmed at any point on the circumference, and all angles are based on the breakpoint or zero point. DP is the jump point between 0 and 360 degrees, for applications with less than 360 degrees of travel, DP should not be set in the same position as the start of the working travel, but must be set outside the working travel.

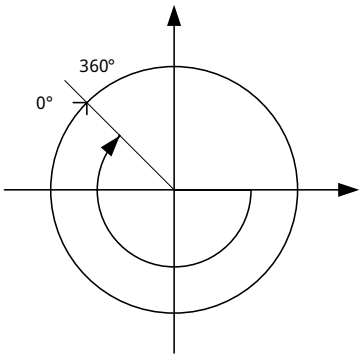


Fig.12 Schematic diagram of DP point

Parameter	Value	Description
DP	0-360	Breakpoint/Zero (Degree)

Direction of Rotation

The CW parameter defines the direction of rotation of the magnet.

Counterclockwise is defined as rotation in 1-4-5-8 pin order (SOP-8 package) or 1-8-9-16 pin order (eTSSOP-16L package); clockwise is defined as the opposite direction, rotation in 8-5-4-1 pin order (SOP-8 package) or 16-9-8-1 pin order (eTSSOP-16L package).

Parameter	Value	Description
CW	0	Counterclockwise
	1	Clockwise

Output Clamp Setting

The output clamp setting is used to limit the output voltage range. CLAMP_LOW sets the minimum output voltage value and CLAMP_HIGH sets the maximum output voltage value. Both parameters work for 4-points, 8-points, 16-points, and 32-points correction modes.

Parameter	Value	Description
CLAMP_LOW	0-100	Clamp Low
CLAMP_HIGH	0-100	Clamp High

4-points Calibration Mode

The SC69401 allows the user to divide the output curve through 4 points into up to 5 segments using the 4-points calibration mode, allowing the number of calibration points to be reduced to 2 or 3. The Y-coordinate (-100%~100%) and X-coordinate (0°~360°) of the 4 calibration points, and the slope of the 5 segments (LNR_S0,LNR_S1,LNR_S2,LNR_S3,LNR_S4) are fully set by the user. To calculate the slope, two endpoints of the curve, 0 degree start and 360 degree end, are needed to calculate LNR_S0 and LNR_D_S.

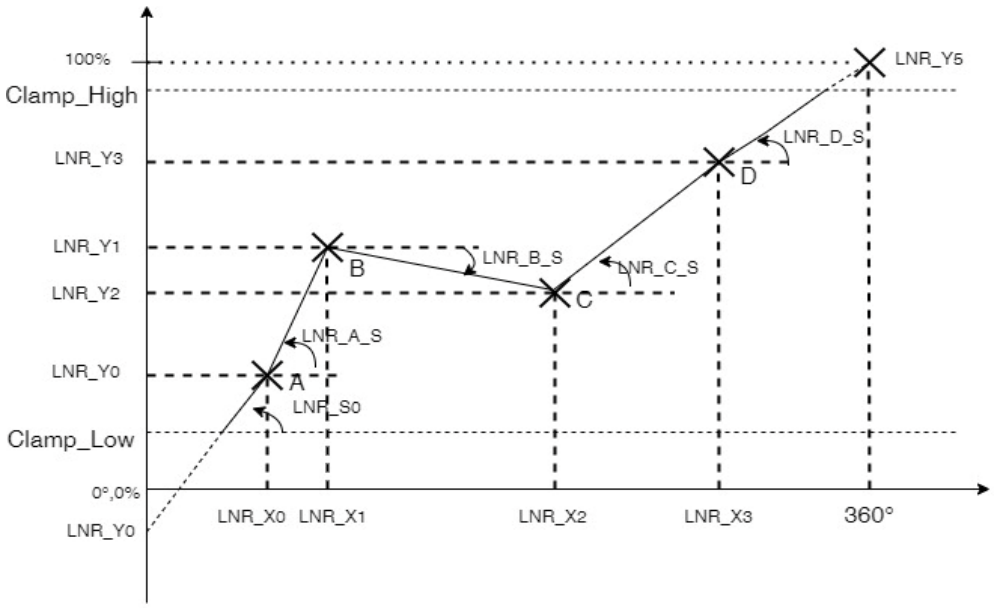


Fig.13 4-points Calibration Curve

8-points Calibration Mode

The SC69401 allows the user to program the output curve desired by the user by customizing the X-coordinate (0°~ 360°) and Y-coordinate (0%~100%) of any 8 calibration points. However, the slope cannot be set and can only be calculated from two neighboring points. A default fixed calibration point [0°, 0%] is also required as a starting point.

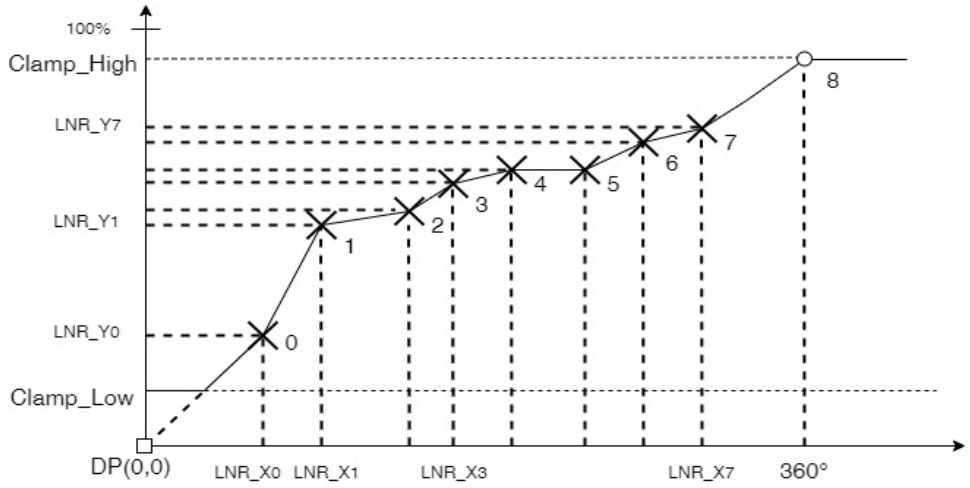


Fig.14 8-points Calibration Curve

16-points Calibration Mode

The 16-points calibration mode allows the user to set only the Y-axis value of the coordinate point. X-axis coordinates are defined by the W value and are divided into 16 segments within the WORK_RANGE range. Y-point coordinates are allowed to range from -50% to +150% of the clamped voltage, which allows the clamped voltage to be in-between a certain segment (as shown in the following figure). But the output is still clamped voltage.

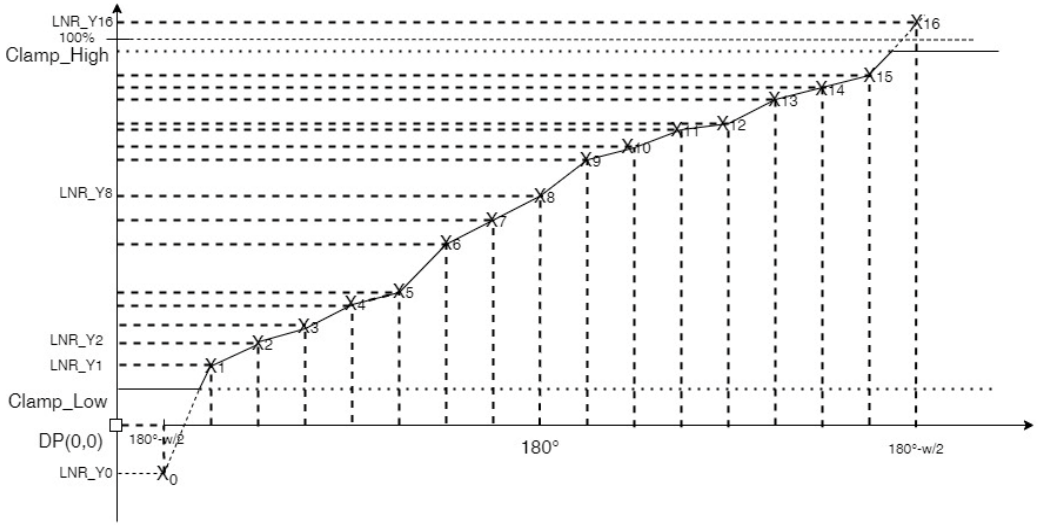


Fig.15 16-points Calibration Curve

32-points Calibration Mode

The work range W is defined by Workrange and is divided into 32 segments centered at 180°. The Y-axis coordinates consist of only 8 bits of data, so they are not absolute values but incremental coordinates. The two endpoints are (180°-w/2, 0%) and (180°+w/2,100%) to define an ideal curve, and ΔY is the fine-tuned value of Y corresponding to the X coordinate of the horizontal axis.

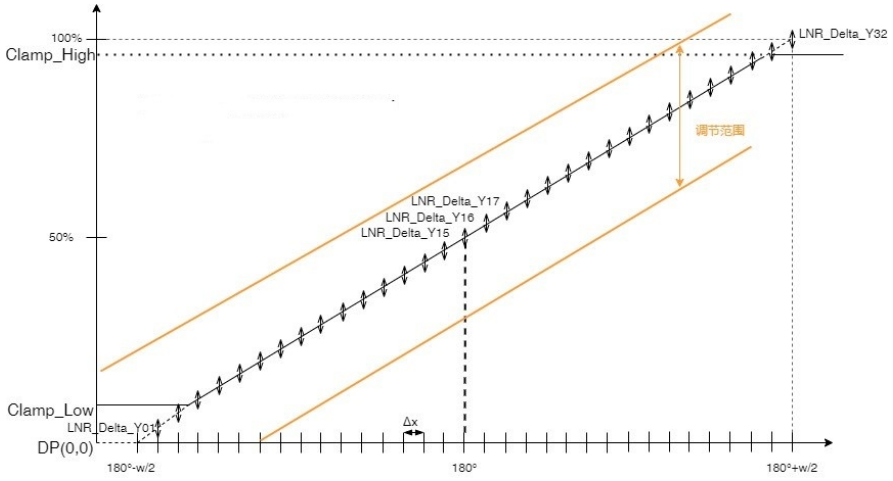


Fig.16 32-points Calibration Curve

32-points, Y-axis coordinate deviation range setting

Parameter	Value	Description
LNR_DELTA_Y_EXPAND【1:0】	0	Tolerance range ±3.125%
	1	Tolerance range ±6.25%
	2	Tolerance range ±12.5%
	3	Tolerance range ±25%

Angle Range Selection

$$w = \frac{WORK\_RANGE\_GAIN \times 360°}{0XFFFF}$$

Angle Range: $\theta_{min} = \frac{360°-w}{2}$ $\theta_{max} = \frac{360°+w}{2}$

θ_{min} indicates the angle at 0% output, and θ_{max} indicates the angle at 100% output. In order to correct the output properly, the angle range needs to be set to an integer multiple greater than 16.

Example of angular range setting:

WORK_RANGE_GAIN	W(°)	Θ_{min}(°)	Θ_{max}(°)	△X，16points(°)	△X，32points(°)
0x1000	22.50034	168.7498	191.2502	1.406271	0.703136
0x1100	23.90661	168.0467	191.9533	1.494163	0.747082
0x1200	25.31289	167.3436	192.6564	1.582055	0.791028
0x1300	26.71916	166.6404	193.3596	1.669947	0.834974
0x2000	45.00069	157.4997	202.5003	2.812543	1.406271
0x2100	46.40696	156.7965	203.2035	2.900435	1.450217
0x2200	47.81323	156.0934	203.9066	2.988327	1.494163
0x2300	49.2195	155.3902	204.6098	3.076219	1.538109

0x3000	67.50103	146.2495	213.7505	4.218814	2.109407
0x3100	68.9073	145.5463	214.4537	4.306706	2.153353
0x3200	70.31357	144.8432	215.1568	4.394598	2.197299
0x3300	71.71984	144.1401	215.8599	4.48249	2.241245
0x4000	90.00137	134.9993	225.0007	5.625086	2.812543
0x4100	91.40764	134.2962	225.7038	5.712978	2.856489
0x4200	92.81392	133.593	226.407	5.80087	2.900435
0x4300	94.22019	132.8899	227.1101	5.888762	2.944381
0xFA00	351.5679	4.216068	355.7839	21.97299	10.9865
0xFB00	352.9741	3.512932	356.4871	22.06088	11.03044
0xFC00	354.3804	2.809796	357.1902	22.14878	11.07439
0xFD00	355.7867	2.106661	357.8933	22.23667	11.11833
0xFE00	357.193	1.403525	358.5965	22.32456	11.16228
0xFF00	358.5992	0.700389	359.2996	22.41245	11.20623
0xFFFF	360	0	360	22.5	11.25

11. Typical Application

Analog/PWM SOP8 Package Application Circuit

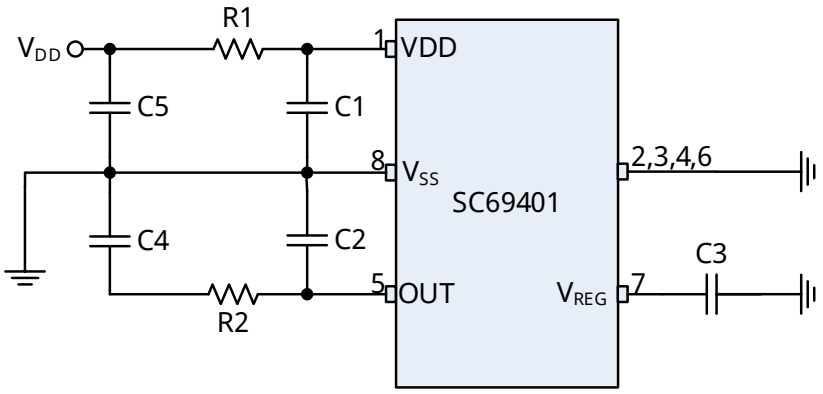


Fig.17 SOP8 Package Application Circuit for Analog/PWM Output

BOM of Analog Output

Component	Min	Typ.	Max	Description
R1	-	0Ω	10Ω	Reduces EMC effects and increases measurement error
R2	-	0Ω	51Ω	Reduces EMC effects
C1	47nF	100nF	-	Placement near pins
C2	47nF	100nF	-	Placement near pins
C3	47nF	100nF	220nF	Placement near pins
C4	-	1nF	10nF	Reduced EMC impact, placed close to the connector end
C5	-	1nF	10nF	Reduced EMC impact, placed close to the connector end

BOM of PWM Output

Component	Min	Typ.	Max	Description
R1	-	0Ω	10Ω	Reduces EMC effects affecting the output high level
R2	-	0Ω	51Ω	Reduces EMC effects, affecting output high and low levels
C1	47nF	100nF	-	Placement near pins
C2	2.2nF	4.7nF	22nF	Placement near pins
C3	47nF	100nF	220nF	Placement near pins
C4	-	-	10nF	Reduced EMC impact, placed close to the connector end
C5	-	1nF	10nF	Reduced EMC impact, placed close to the connector end

Analog/PWM eTSSOP-16L Package Application Circuit

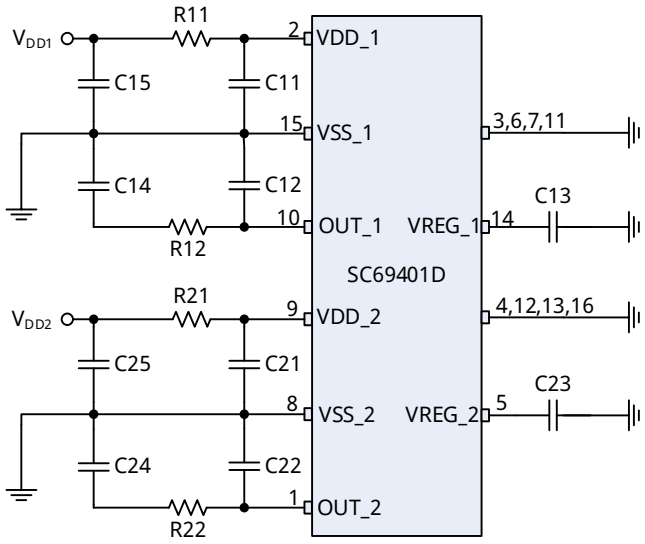


Fig.18 eTSSOP-16L Package Application Circuit for Analog/PWM Output

BOM of Analog Output

Component	Min	Typ.	Max	Description
R11, R21	-	0Ω	10Ω	Reduces EMC effects and increases measurement error
R12, R22	-	0Ω	51Ω	Reduces EMC effects and increases measurement error
C11, C21	47nF	100nF	-	Placement near pins
C12, C22	47nF	100nF	-	Placement near pins
C13, C23	47nF	100nF	220nF	Placement near pins
C14, C24	-	1nF	10nF	Reduced EMC impact, placed close to the connector end
C15, C25	-	1nF	10nF	Reduced EMC impact, placed close to the connector end

BOM of PWM Output

Component	Min	Typ.	Max	Description
R11, R21	-	0Ω	10Ω	Reduces EMC effects affecting the output high level
R12, R22	-	0Ω	51Ω	Reduces EMC effects, affecting output high and low levels
C11, C21	47nF	100nF	-	Placement near pins
C12, C22	2.2nF	4.7nF	22nF	Placement near pins
C13, C23	47nF	100nF	220nF	Placement near pins
C14, C24	-	-	10nF	Reduced EMC impact, placed close to the connector end
C15，C25	-	1nF	10nF	Reduced EMC impact, placed close to the connector end

SPI SOP8 Package Application Circuit

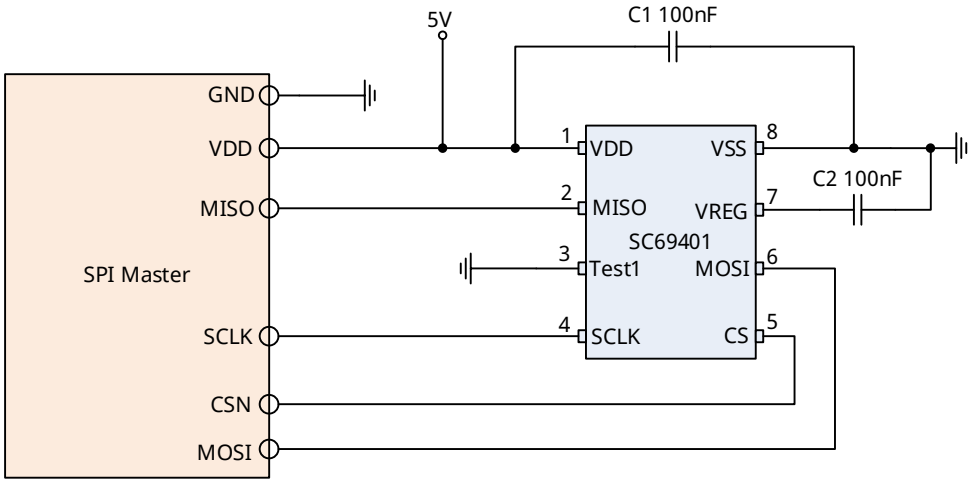


Fig.19 SOP8 Package Application Circuit for SPI Output

SPI eTSSOP-16L Package Application Circuit

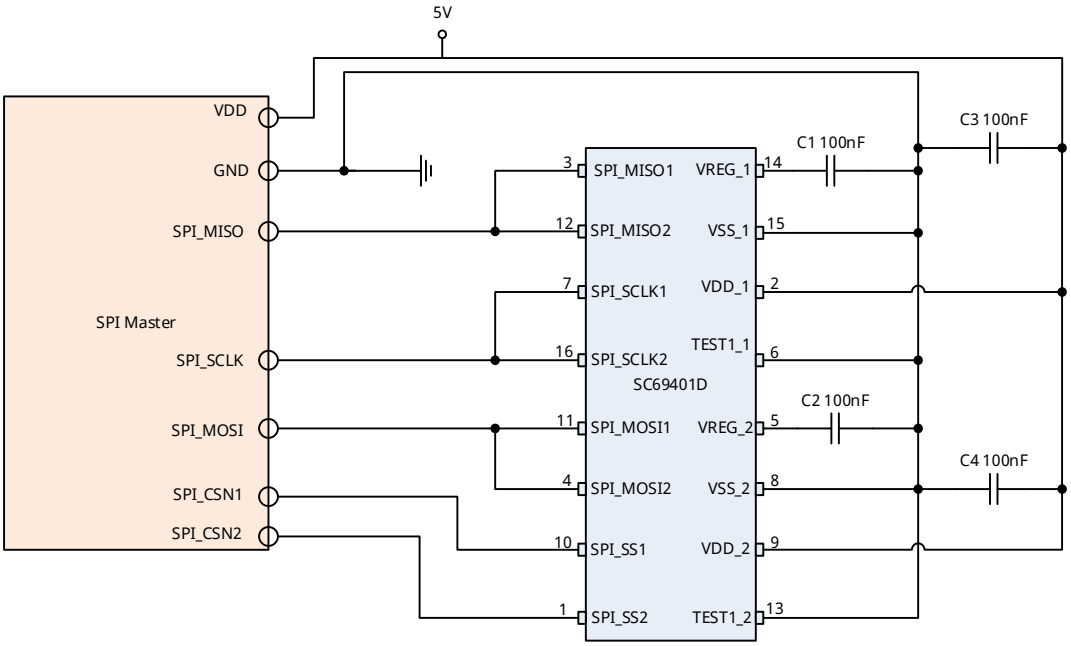
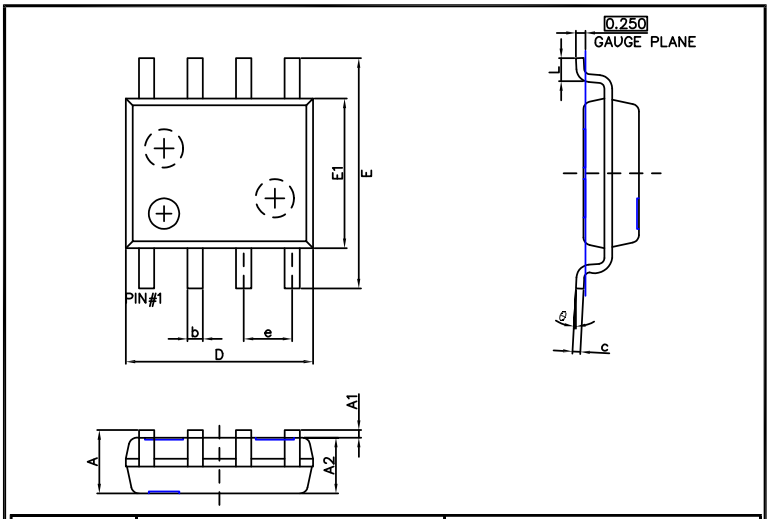


Fig.20 eTSSOP-16L Package Application Circuit for SPI Output

12. Package Information

SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Fig.21 SOP8 Package Dimensions

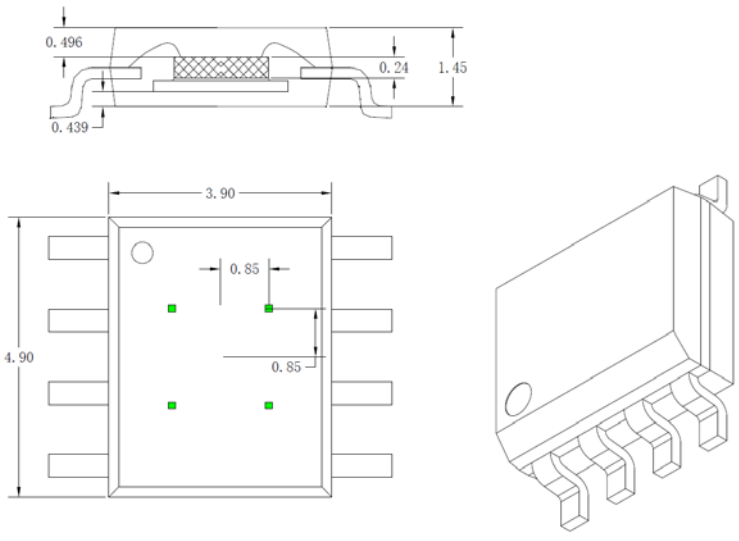
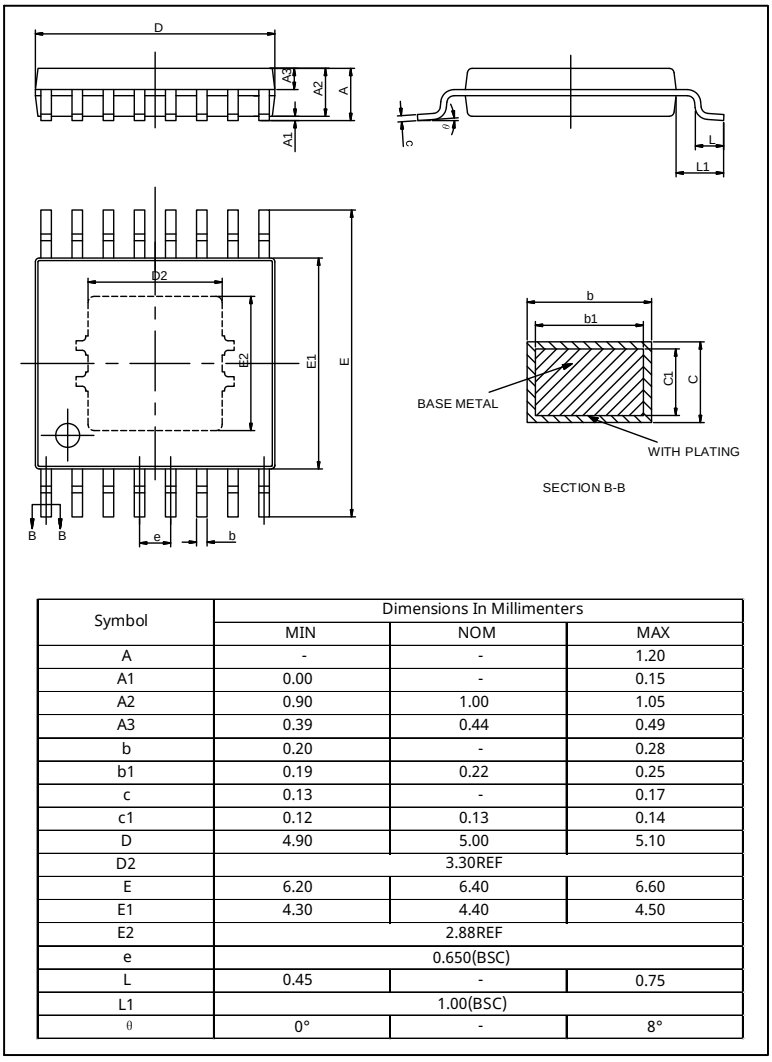


Fig.22 Hall Plate Location for SOP8 Package

eTSSOP-16L



Symbol	Dimensions In Millimenters		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.00	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
D2		3.30REF	
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2		2.88REF	
e		0.650(BSC)	
L	0.45	-	0.75
L1		1.00(BSC)	
θ	0°	-	8°

Fig.23 eTSSOP-16L Package Dimensions

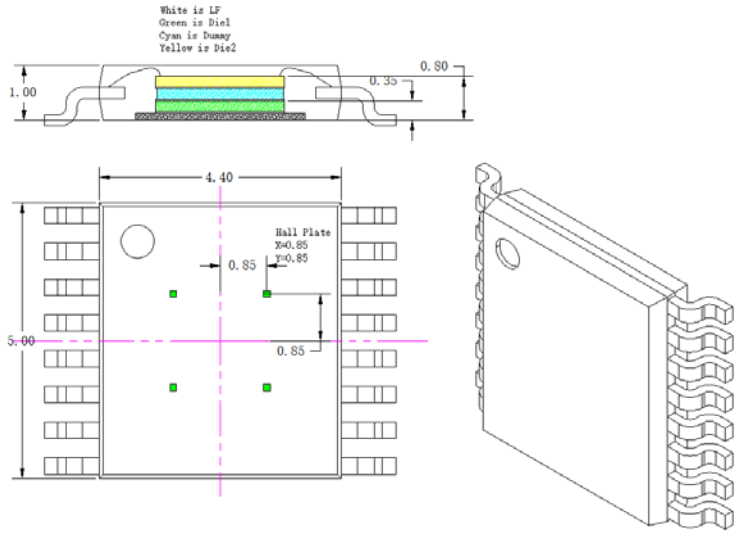


Fig.24 Hall Plate Location for eTSSOP-16L Package

13. Revision History

Revision	Date	Description
Rev.E0.1	2023-07-23	Initial revision
Rev.A1.0	2024-02-30	Release of official version
Rev.A1.1	2024-06-21	1, SOP-8 package quantity updated to 4000 pcs/reel 2, Change the active diagnostic output voltage limit 3, Diagnostic mask register BIT1 add ADC overflow mask 4, 4-point calibration Y-axis coordinate value is updated to -100% 5, Update the capacitor and resistor matching value of the proposed schematic diagram 6, Update the information of hall plate
Rev.A1.2	2025-01-22	Update ordering information