4V-60V Input Current Mode Synchronous Buck Controller

DESCRIPTION

The VE8600 is a high-voltage, synchronous, step-down controller. The VE8600 uses current mode control with cycle-by-cycle peak valley current limiting or hiccup mode OCP.

The VE8600 has DEM (diode emulation mode) that optimizes light-load efficiency.

The operating frequency of the VE8600 can be programmed by an external resistor or synchronized to an external clock from 100kHz to 1MHz.

The VE8600 offers programmable soft-start and power-good indicator. Full protection features include precision output over-voltage protection (OVP), output over-current protection (OCP), and thermal shutdown.

The VE8600 offers shunt or DCR current sense scheme to detect instant inductor current. The instant peak and valley inductor current limit function is then implemented, which can offer constant current charging for a battery or supper capacitor.

The VE8600 is available in TSSOP20-EP and QFN3X4-20(3mm x 4mm Wettable Flank) packages. Both packages use EPAD to improve thermal performance and noise immunity. Low pin count, fewer external components, and default internal values make VE8600 an ideal solution for time to market simple power supply design.

Automotive-compliant parts are available under separate datasheet (VE8600Q).

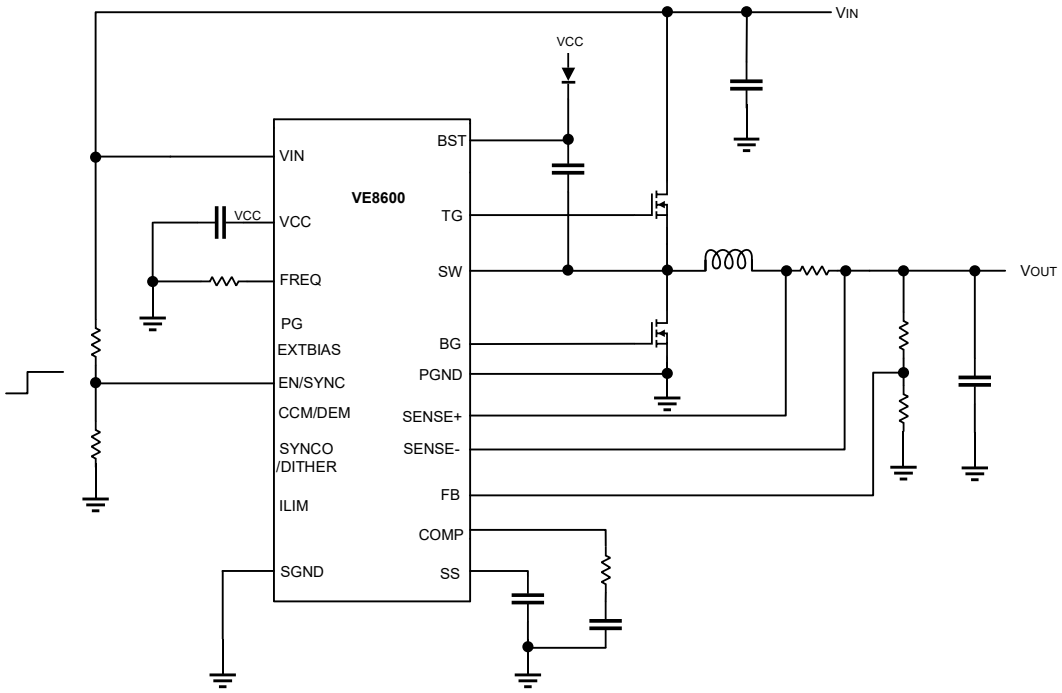
FEATURES

- Wide 4V to 60V Operating Input Range
- Wide 0.8V to 60V Operating Output Range
- Dual N-Channel MOSFET Driver
- 0.8V Voltage Reference with ±1.5% Accuracy Over Temperature
- Low Dropout Operation: Maximum Duty Cycle at 99.5%
- Programmable Frequency Range: 100kHz - 1MHz
- External Sync Clock Range: 100kHz-1MHz
- 180º Out-of-Phase SYNCO Pin and Dither
- Programmable Soft Start (SS)
- Power Good (PG) Output Voltage Monitor
- Selectable Cycle-by-Cycle Current Limit
- Output Over-Voltage Protection (OVP)
- Hiccup Mode Over-Current Protection
- Peak Valley Current Limit
- Internal LDO with External Power Supply Option
- Programmable CCM and DEM Mode
- Shunt and DCR Sensing
- Low Side FET Ron Sense ZCD
- Available in TSSOP20-EP and QFN3X4-20 (3mm x 4mm Wettable Flank) Packages

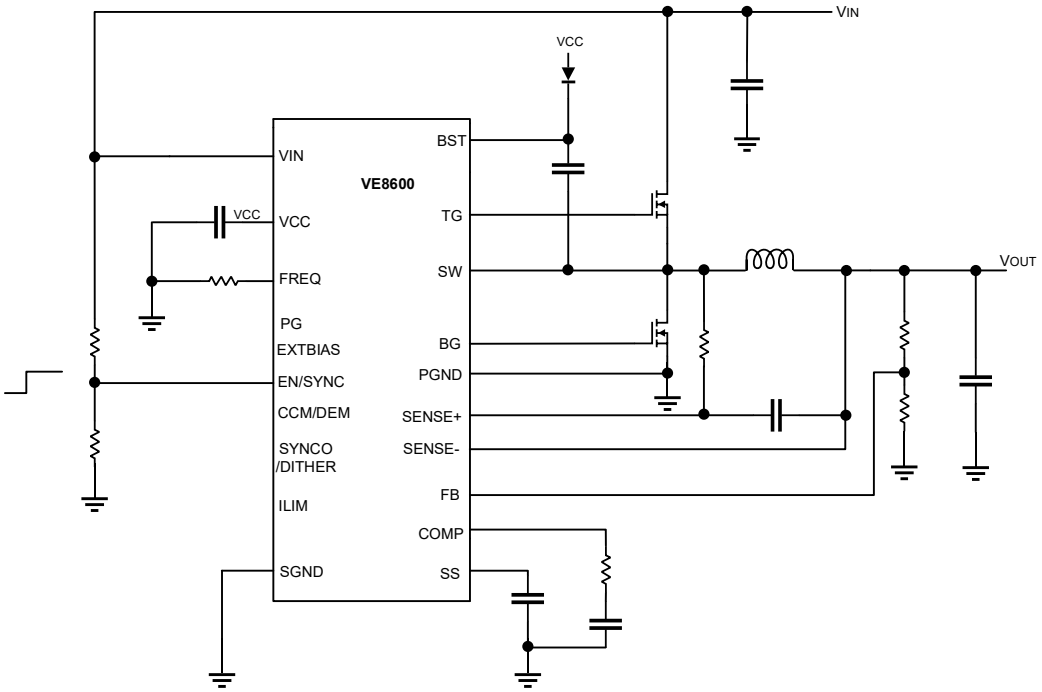
APPLICATIONS

- Automotive
- Industrial
- Renewable energy
- Redundant power supplies
- Robot and drones

TYPICAL APPLICATION

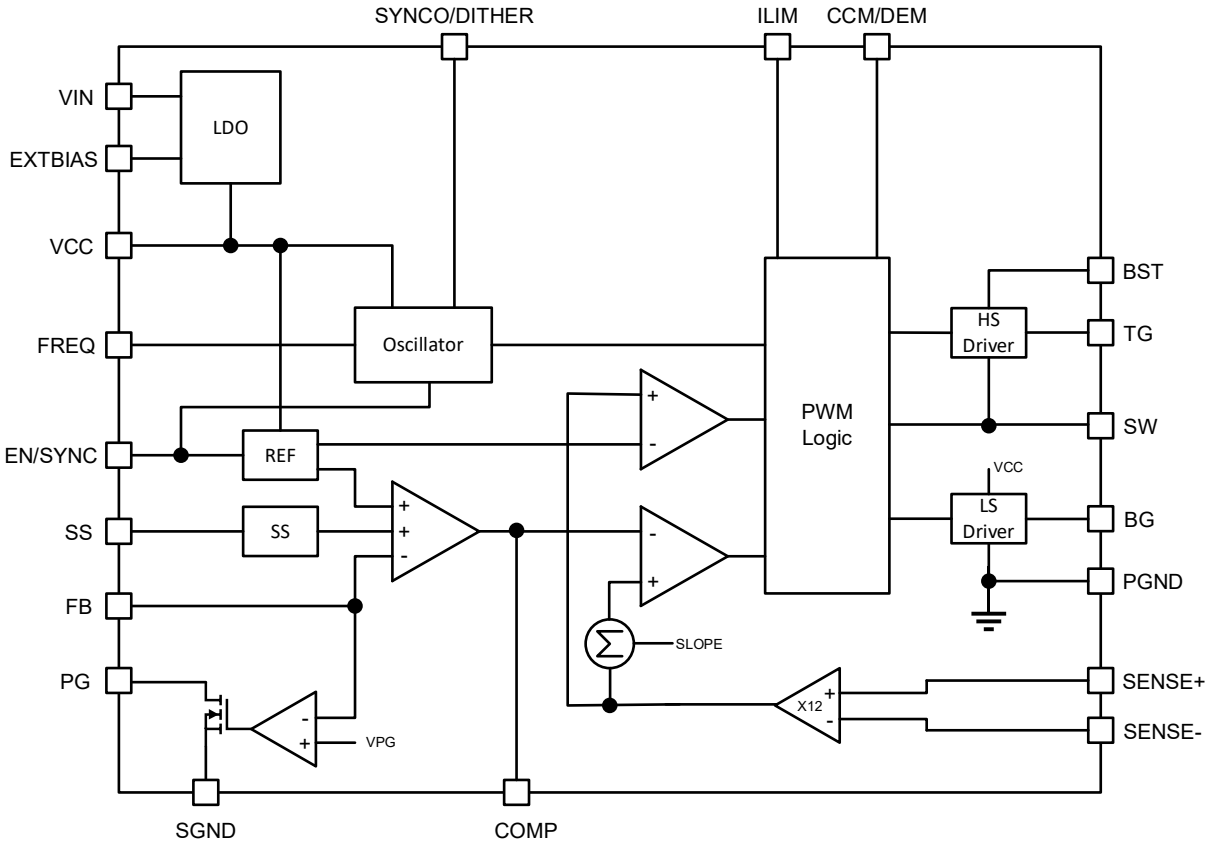


Shunt Sensing Application



DCR Sensing Application

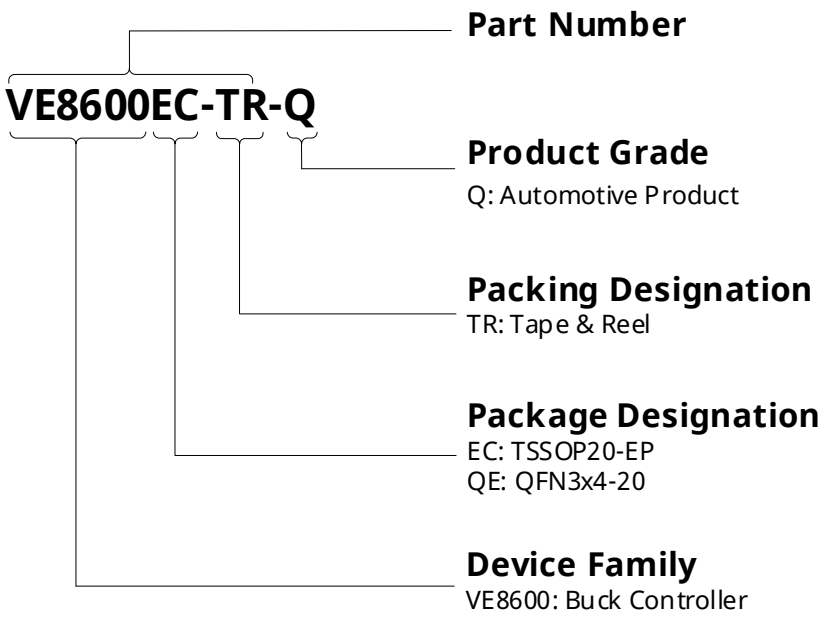
BLOCK DIAGRAM



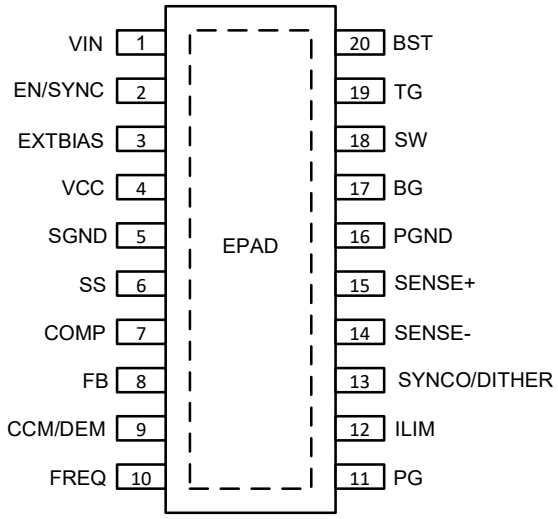
ORDERING INFORMATION

Ordering Information	Mark	Class (1)	Temperature Range	Package	Pack	Quantity
VE8600EC-TR	8600	I	-40 to +125°C	TSSOP20-EP	TR	4000
VE8600QE-TR	8600	I	-40 to +125°C	QFN3x4-20	TR	5000
VE8600EC-TR-Q	8600	Q	-40 to +125°C	TSSOP20-EP	TR	4000
VE8600QE-TR-Q	8600	Q	-40 to +125°C	QFN3x4-20	TR	5000

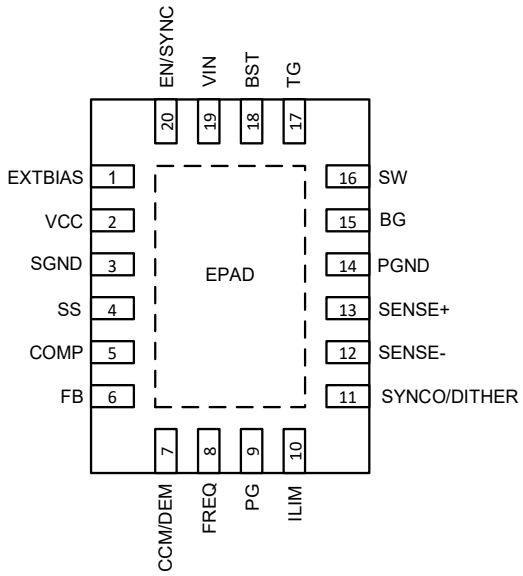
Note 1: The Class definition, Q=Automotive, I=Industrial.



PIN CONFIGURATIONS



TSSOP20-EP



QFN3x4-20

PIN DESCRIPTION

Name	TSSOP20-EP	QFN3X4-20	Description
VIN	1	19	**Input supply.** This pin should be tied to input rail. Decouple this pin with a small ceramic capacitor to ground.
EN/SYNC	2	20	**Enable input.** The threshold is 1.2V with 120mV of hysteresis and is used to implement an input under-voltage lockout (UVLO) function externally. If an external sync clock (the frequency is higher than default frequency set by FREQ) is applied to EN/SYNC, the internal clock follows the sync frequency.
EXTBIAS	3	1	**External power supply for the internal VCC regulator**. EXTBIAS disables the power from VIN for as long as EXTBIAS is higher than 4.7V. Do not connect a power supply greater than 24V to EXTBIAS. Connect EXTBIAS to an external power supply to reduce power dissipation and increase efficiency.
VCC	4	2	**Internal bias supply.** 5V internal bias supply. A≥4.7μF decoupling capacitor is required between VCC and PGND.
SGND	5	3	**Low-noise ground reference.** SGND should be connected to the ground side of the output capacitors.

Name	TSSOP20-EP	QFN3X4-20	Description
SS	6	4	**Soft-start control input.** SS is used to program the soft-start period with an external capacitor between SS and SGND.
COMP	7	5	**Regulation control loop compensation.** Connect an RC network from COMP to SGND to compensate for the regulation control loop.
FB	8	6	**Feedback.** Connect FB to a resistor voltage divider from the output to ground.
CCM/DEM	9	7	**Continuous conduction mode/Diode emulation mode (DEM).** Floating CCM/DEM or connecting CCM/DEM to VCC makes the part operate in CCM. Connecting an appropriate external resistor from CCM/DEM to SGND makes the part operate in DEM mode. The DEM voltage should be no less than 300mV.
FREQ	10	8	**Frequency.** Connect a resistor between FREQ and SGND to set the switching frequency.
PG	11	9	**Power good output.** The output of PG is an open drain.
ILIM	12	10	**Sense voltage limit set.** The voltage at ILIM sets the nominal sense voltage at the maximum output current. There are three fixed options: float, VCC, and SGND. Connect a resistor or a voltage source that is higher than 0.64V and lower than 1.5V to enable the constant current mode.
SYNCO/ DITHER	13	11	**Frequency synchronous out.** SYNCO outputs a 180° out-of-phase clock when the part works in CCM for dual-channel operation. Connect to GND to enable the dither.
SENSE-	14	12	**Negative input for the current sense.** The sensed inductor current limit threshold is determined by the status of ILIM.
SENSE+	15	13	**Positive input for the current sense.** The sensed inductor current limit threshold is determined by the status of ILIM.
PGND	16	14	**Power ground.** Connect PGND directly to the negative terminal of the VCC decoupling capacitor.
BG	17	15	**Bottom gate driver output.** Connect BG to the gate of the bottom MOSFET.
SW	18	16	**Switch node.** SW is the reference for the V_{BST} supply and high-current returns for the bootstrapped switch.
TG	19	17	**Top gate drive.** TG drives the gate of the top MOSFET. The TG driver draws power from the BST capacitor and returns to SW, providing a true floating drive to the top N-

Name	TSSOP20-EP	QFN3X4-20	Description
			channel MOSFET.
BST	20	18	**Bootstrap.** BST is the positive power supply for the high-side MOSFET driver. Connect a bypass capacitor between BST and SW. A Schottky or high-speed diode must be tied from VCC to BST.
EPAD			**Exposed pad.** The exposed pad is on the bottom side of device. It is not electrically connected to SGND or PGND. Connect the exposed pad to SGND and PGND during PCB layout for better thermal performance.

ABSOLUTE MAXIMUM RATINGS

Parameter	Minimum	Maximum	Unit
VIN	-0.3	+65	V
SW	-0.3	+65	V
SW (transient < 20 ns)	-5	+65	V
BST to SW	-0.3	VCC+0.3	V
TG to SW	-0.3	VCC+0.3	V
EN / SYNC	-0.3	+65	V
VCC	-0.3	+6.5	V
EXTBIAS	-0.3	+26	V
SENSE+-	-0.3	+65	V
SENSE+ to SENSE-	-0.3	+0.3	V
All Other Pins	-0.3	VCC+0.3	V
Junction Temperature		+150	°C

ESD RATINGS

Parameter	Value	Unit
Human Body Model (HBM), per AEC-Q100-002	2	kV
Charged Device Model (CDM), per AEC-Q100-011	1	kV
Latch-Up, per AEC-Q100-004	100	mA

THERMAL INFORMATION

Thermal Resistance	θ_{JA}(°C/W)	θ_{JC}(°C/W)
TSSOP20-EP	40	8
QFN-20	48	10

RECOMMENDED OPERATINIG CONDITIONS

Parameter	Minimum	Maximum	Unit
Temperature	-40	+125	°C
VIN to GND	+4	+60	V
EN / SYNC	0	+60	V
SENSE+,SENSE- to GND	0	+60	V
EXTBIAS to GND	+4.7	+24	V

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 2V, $V_{EXTBIAS}$ = 0V, V_{ILIM} = Floating, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Supply						
V_{IN} UVLO threshold (rising)	$V_{IN\_UV\_RISING}$			4.08		V
V_{IN} UVLO threshold (falling)	$V_{IN\_UV\_FALLING}$			3.78		V
V_{IN} UVLO hysteresis	$V_{IN\_UV\_HYS}$			300		mV
V_{IN} supply current with EXTBIAS bias	$I_{Q\_EXTBIAS}$	EXTBIAS = 12V, $V_{CCM/DEM}$ = 5V, V_{FB} = 0.84V, SENSE+ = SENSE- = 0V, no switching		10		μA
V_{IN} supply current without EXTBIAS bias	I_Q	EXTBIAS = 0V, V_{FB} = 0.84V, $V_{CCM/DEM}$ = 5V, SENSE+ = SENSE- = 0V, no switching		1600		μA
V_{IN} DEM current	I_{Q_DEM}	EXTBIAS = 0V, $V_{CCM/DEM}$ = 0.6V, V_{FB} = 0.84V,SENSE+ = SENSE- = 12V,no switching		500		μA
V_{IN} shutdown current	I_{SHDN}	V_{EN} = 0V		5	15	μA
VCC Regulator						
VCC regulator output voltage from V_{IN}	VCC_{VIN}	V_{IN} > 6V, I_{LOAD} = 0 to 50mA	4.75	5	5.25	V
VCC regulator load regulation from V_{IN}		I_{LOAD} = 0 to 50mA, EXTBIAS floating or connected to SGND		2	5	%
VCC regulator output voltage from EXTBIAS	$VCC_{EXTBIAS}$	EXTBIAS > 6V	4.75	5	5.25	V
VCC regulator load regulation from EXTBIAS		I_{LOAD} = 0 to 50mA, EXTBIAS = 12V		1	3	%
EXTBIAS UVLO threshold (rising)	EXTBIAS_RISING		4.3	4.68	4.92	V
EXTBIAS UVLO threshold (falling)	EXTBIAS_FALLING		4.05	4.42	4.75	V
EXTBIAS threshold hysteresis	EXTBIAS_HYS			258	278	mV
EXTBIAS supply current	$I_{EXTBIAS}$	V_{DEM} = 5V, V_{FB} = 0.84V, SENSE+ = SENSE- = 12V, EXTBIAS = 12V,no switching		960		μA
		V_{DEM} = 0.6V, V_{FB} = 0.84V, SENSE+ = SENSE- = 12V, EXTBIAS = 12V,no switching		500		μA
Feedback (FB)						

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Feedback voltage	V_{FB}	4V < V_{IN} < 60V	0.788	0.8	0.812	V
Feedback current	I_{FB}	V_{FB} = 0.8V		10		nA
Enable (EN/SYNC)						
Enable threshold (rising)	V_{EN_RISING}			1.2	1.25	V
Enable threshold (falling)	$V_{EN\_FALLING}$			1.08		V
Enable threshold hysteresis	V_{EN_TH}			120		mV
Enable input current	I_{EN}	V_{EN} = 2V		1	2	μA
Enable turn-off delay	T_{OFF}		18	42	72	μs
Oscillator and Sync						
Operating frequency	F_{SW}	R_{FREQ} = 90 kΩ		500		kHz
Foldback operating frequency	$F_{SW\_FOLDBACK}$	V_{FB} = 0.1V		50%		F_{SW}
Maximum frequency	F_{SWH}		1000			kHz
Minimum frequency	F_{SWL}				100	kHz
EN/SYNC frequency range	F_{SYNC}		100		1000	kHz
EN/SYNC voltage rising threshold	V_{SYNC_RISING}		2			V
EN/SYNC voltage falling threshold	$V_{SYNC\_FALLING}$				0.35	V
Current Sense						
Current sense common mode voltage range	$V_{SENSE+/-}$		0		65	V
Current limit sense voltage	V_{ILIMIT}	ILIM = SGND, V_{SENSE+} = 12V	14	24	34	mV
		ILIM = VCC, V_{SENSE+} = 12V	39	49	59	
		ILIM = FLOAT, V_{SENSE+} = 12V	64	74	84	
Reverse current limit sense voltage	V_{REV_ILIMIT}	ILIM = SGND, V_{SENSE+} = 12V		8		mV
		ILIM = VCC, V_{SENSE+} = 12V		16		
		ILIM = FLOAT, V_{SENSE+} = 12V		25		
Valley current limit	V_{VAL_ILIMIT}	ILIM = SGND, V_{SENSE+} = 12V		14.5		mV
		ILIM = VCC, V_{SENSE+} = 12V		41.5		
		ILIM = FLOAT, V_{SENSE+} = 12V		66.5		
Input current of sensor	I_{SENSE+}	V_{SENSE+} = V_{SENSE-} = 12V			1	uA
		V_{SENSE+} = V_{SENSE-} = 1V			1	
	I_{SENSE-}	V_{SENSE+} = V_{SENSE-} = 12V	240	270	300	uA
		V_{SENSE+} = V_{SENSE-} = 1V			1	
Soft Start (SS)						
Soft-start source current	I_{SS}	SS = 0.5V	2	4	6	μA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Error Amplifier (EA)						
Error amp transconductance	G_M	ΔV = 5mV	420	550	720	μS
Error amp open loop DC gain	A_O		70	75	82	dB
Error amp sink/source current	I_{EA}	FB = 0.7/0.9V		±50		μA
Protection						
Over-voltage threshold	V_{OV}		110%	116%	120%	V_{FB}
Over-voltage hysteresis	V_{OV_HYS}			3%		V_{FB}
Thermal shutdown				170		°C
Thermal shutdown hysteresis				20		°C
Gate Driver						
TG pull-up resistor	R_{TG_PULLUP}			2		Ω
TG pull-down resistor	R_{TG_PULLDN}			1		Ω
BG pull-up resistor	R_{BG_PULLUP}			2		Ω
BG pull-down resistor	R_{BG_PULLDN}			1		Ω
Dead time	T_{DEAD}			20		ns
TG maximum duty cycle	D_{MAX}	V_{FB} = 0.7V	98	99.3		%
TG minimum on time	$T_{ON\_MIN\_TG}$			170		ns
BG minimum on time	$T_{ON\_MIN\_BG}$			145		ns
Power Good (PG)						
Power good low	V_{PG_LOW}	I_{LOAD} = 4mA		0.2	0.3	V
PG rising threshold	PG_{VTH_RSING}	V_{OUT} rising		90%		V_{FB}
		V_{OUT} falling		110%		V_{FB}
PG falling threshold	$PG_{VTH\_FALLING}$	V_{OUT} falling		88%		V_{FB}
		V_{OUT} rising		112%		V_{FB}
PG threshold hysteresis	PG_{VTH_HYS}			2%		V_{FB}
Power good leakage	I_{PG_LK}	PG = 5V			2	μA
Power good delay	T_{PG_DELAY}	Rising		70		μs
		Falling		55		
DEM Mode/CCM						
DEM mode output current	I_{DEM}	R_{FREQ} = 90 kΩ		6.5		μA
CCM required DEM threshold voltage	V_{CCM_TH}		3			V

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

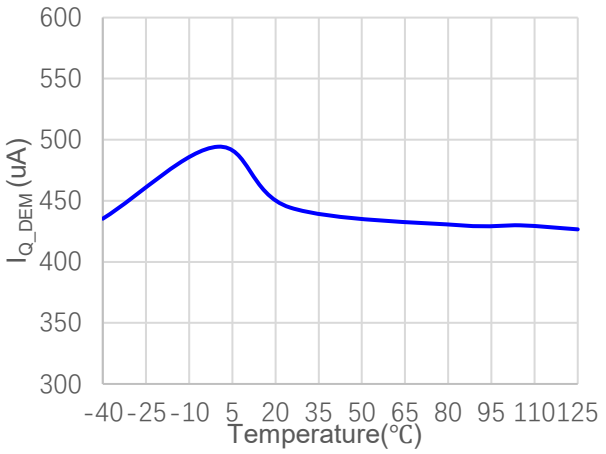


Figure 1. I_{Q_DEM} vs Temp

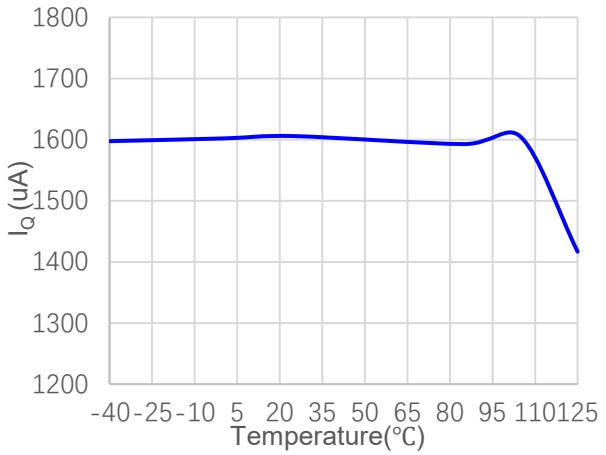


Figure 2. I_Q vs Temp

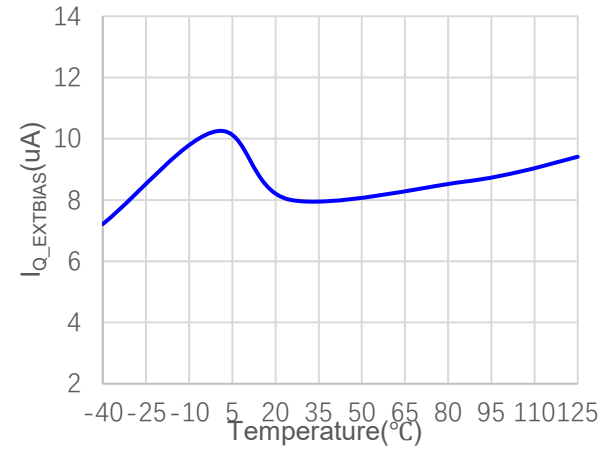


Figure 3. $I_{Q\_EXTBIAS}$ vs Temp

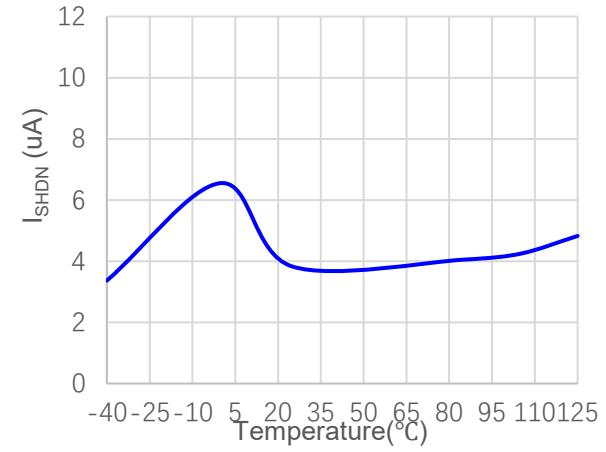


Figure 4. I_{SHDN} vs Temp

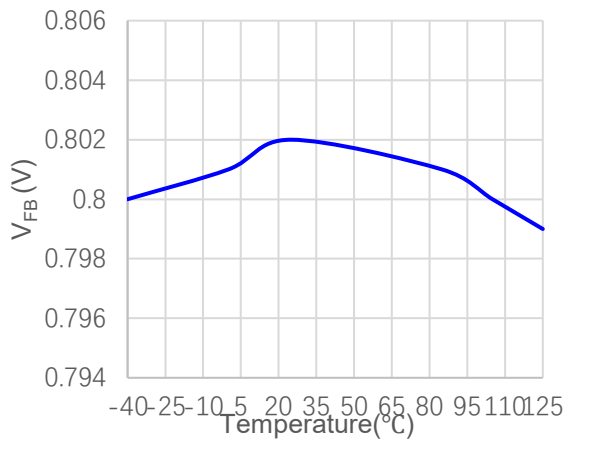


Figure 5. V_{FB} vs Temp

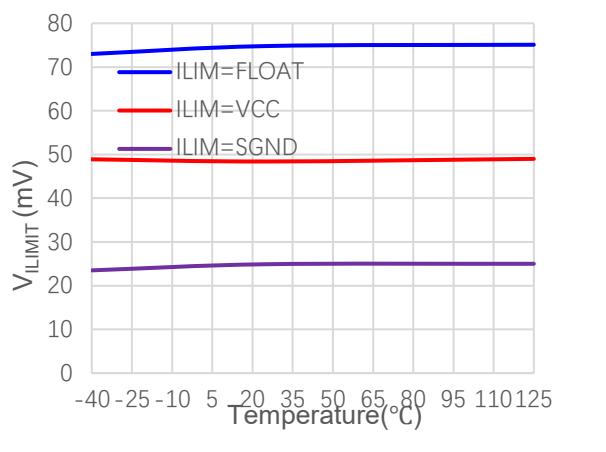


Figure 6. V_{ILIMIT} vs Temp

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

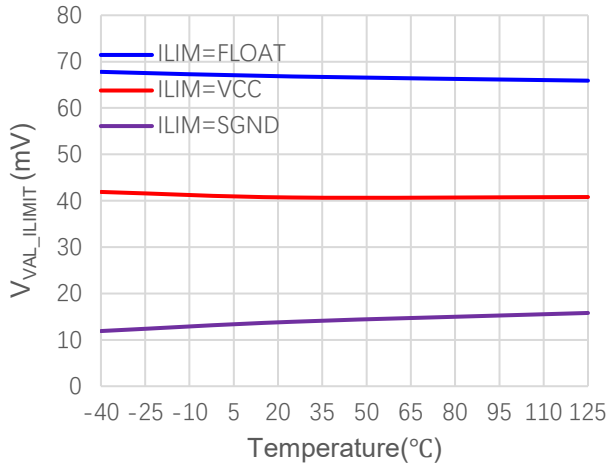


Figure 7. V_{VAL_ILIMIT} vs Temp

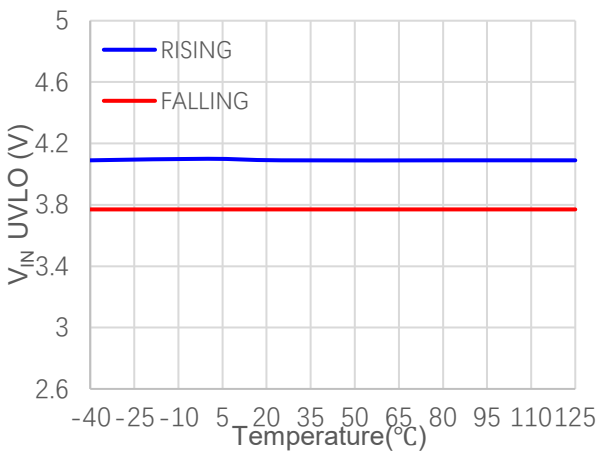


Figure 8. V_{IN} UVLO vs Temp

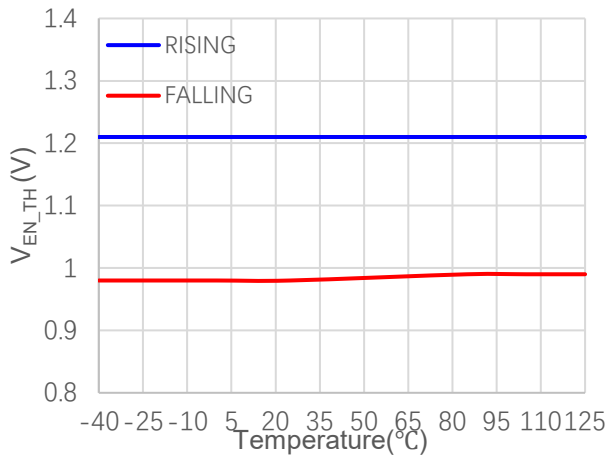


Figure 9. V_{EN_TH} vs Temp

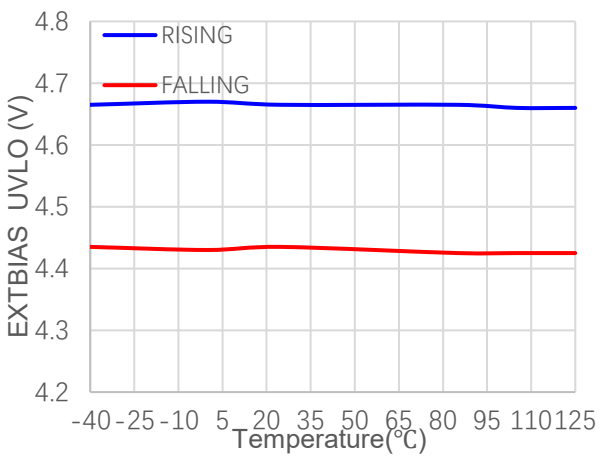


Figure 10. EXTBIAS UVLO vs Temp

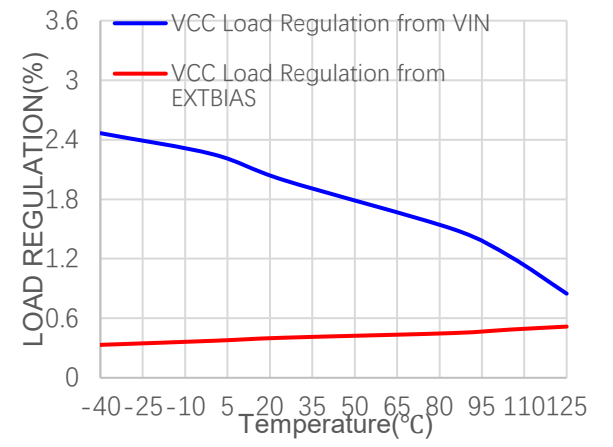


Figure 11. VCC Load Regulation vs Temp

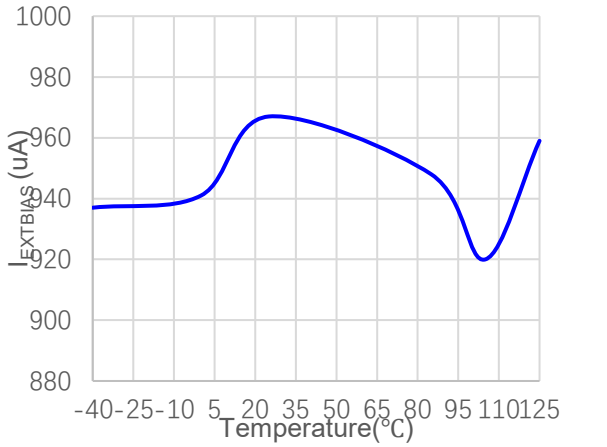


Figure 12. $I_{EXTBIAS}$ with 5V vs Temp

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted

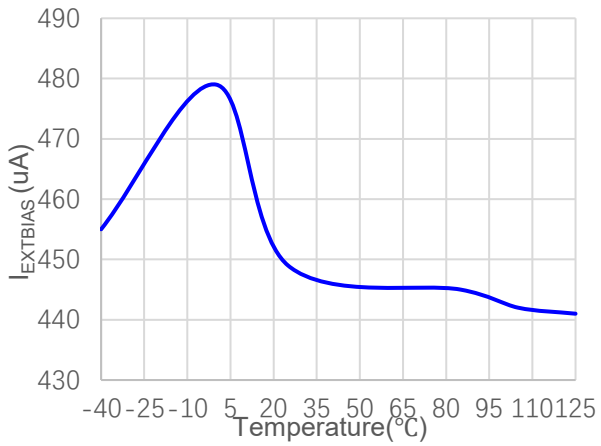


Figure 13. $I_{EXTBIAS}$ with DEM 600mV vs Temp

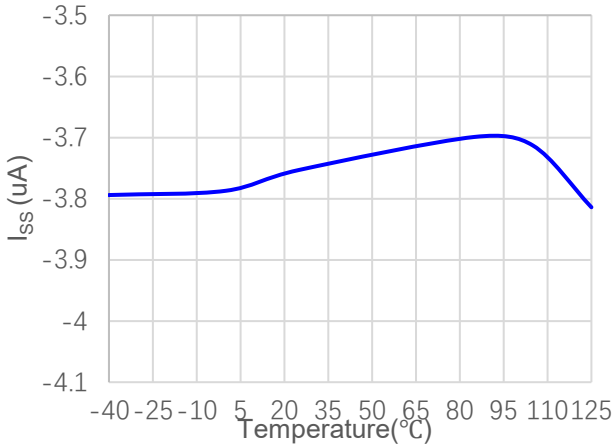


Figure 14. I_{SS} vs Temp

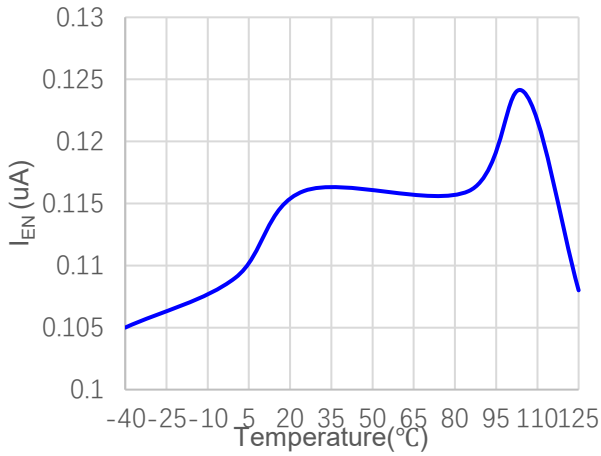


Figure 15. I_{EN} vs Temp

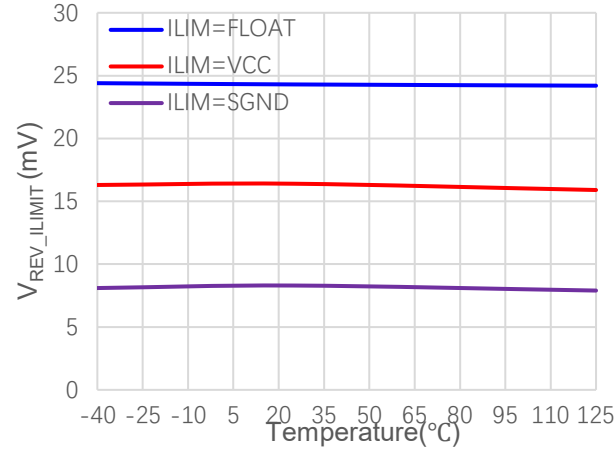


Figure 16. V_{REV_ILIMIT} vs Temp

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, F_{sw} = 300 kHz, T_J = -40°C to +125°C, unless otherwise noted.

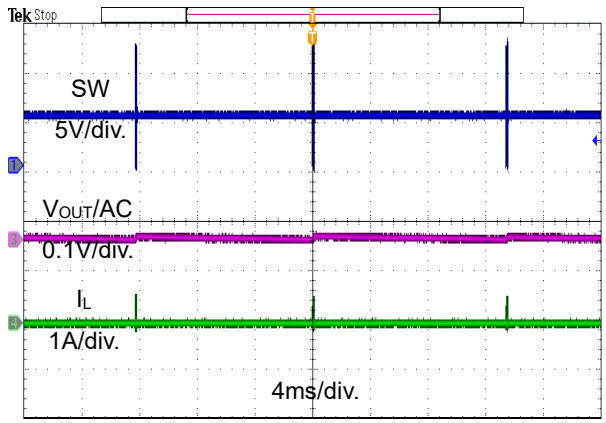


Figure 17. Steady State I_{OUT}=0A DEM

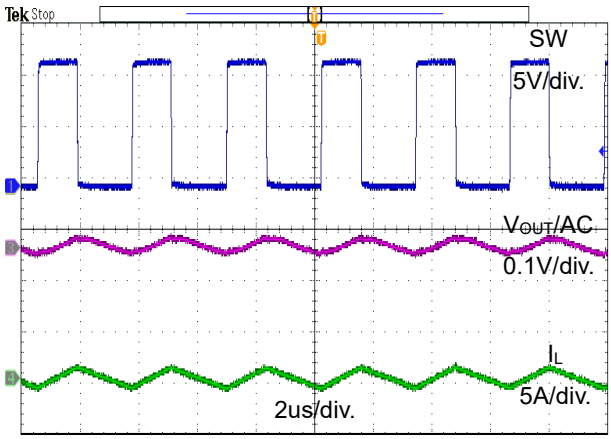


Figure 18. Steady State I_{OUT}=0A CCM

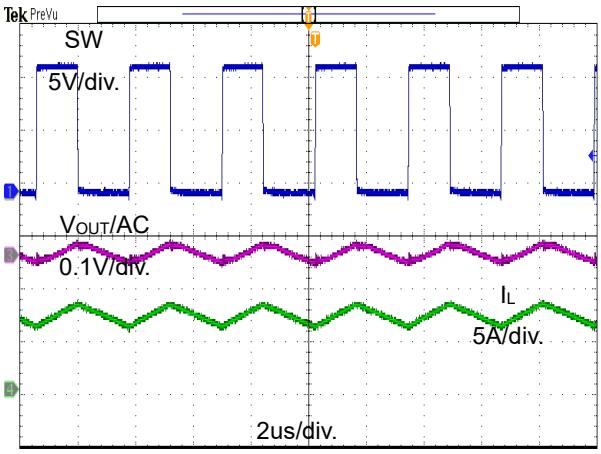


Figure 19. Steady State I_{OUT}=7A CCM

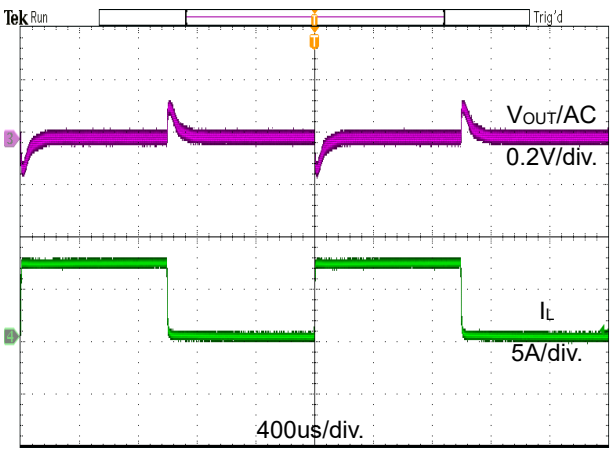


Figure 20. Dynamic Load I_{OUT}=0-7A CCM

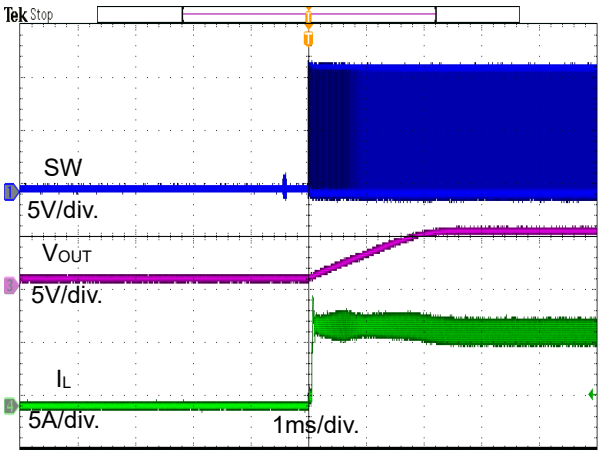


Figure 21. Start Up I_{OUT}=7A CCM

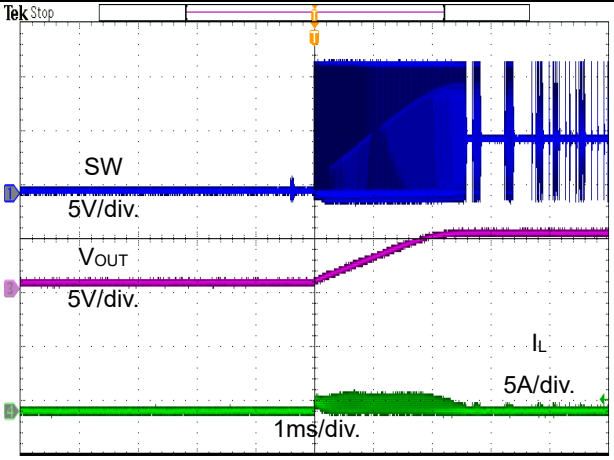


Figure 22. Start Up I_{OUT}=0A DEM

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=5V, F_{sw}=300 kHz, T_J = -40°C to +125°C, unless otherwise noted.

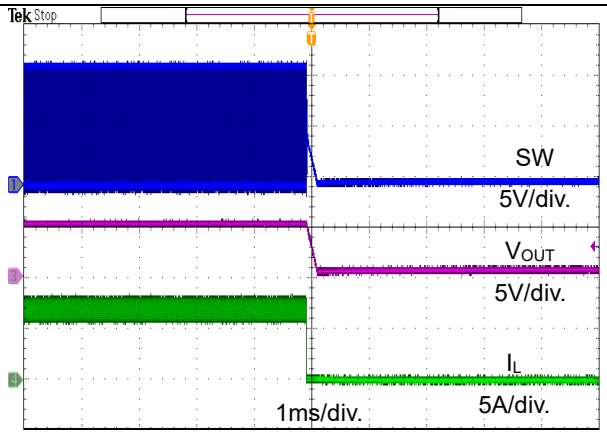


Figure 23. Shut Down Through EN/SYNC I_{OUT}=7A

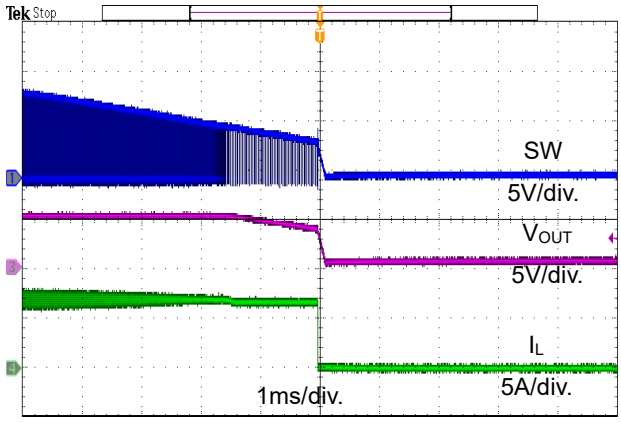


Figure 24. Shut Down Through VIN I_{OUT}=7A

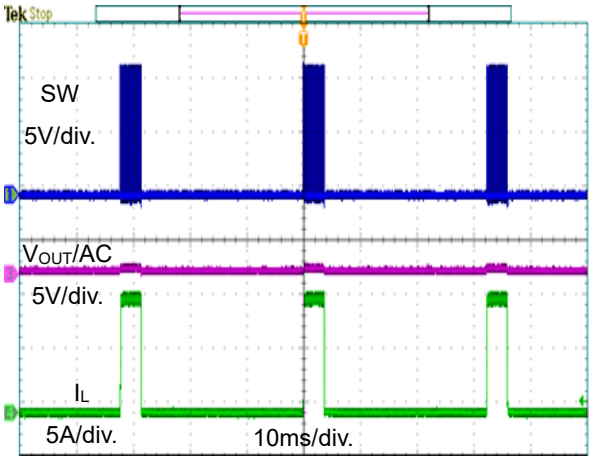


Figure 25. Hiccup OCP

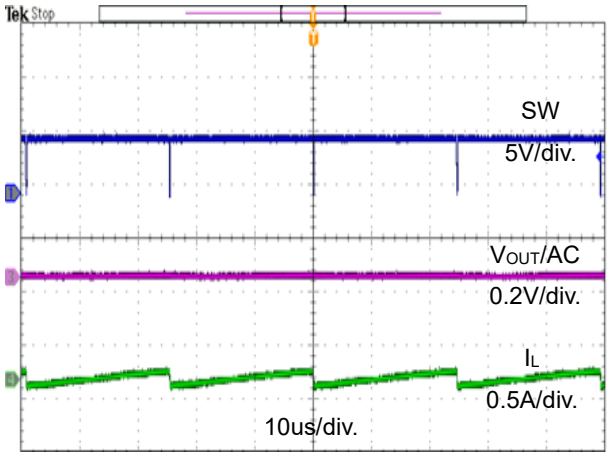


Figure 26. Low Dropout Mode

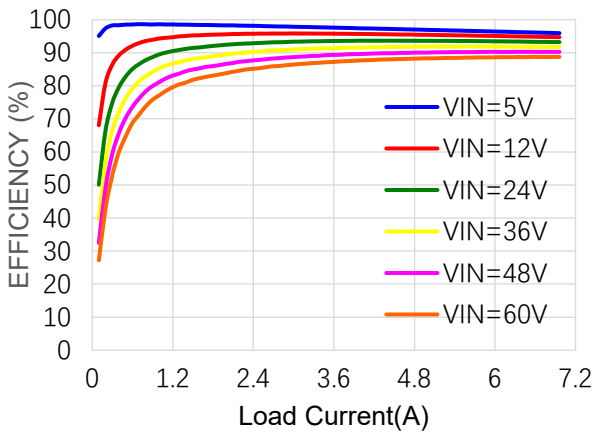


Figure 27. Efficiency vs Load Current at 25°C

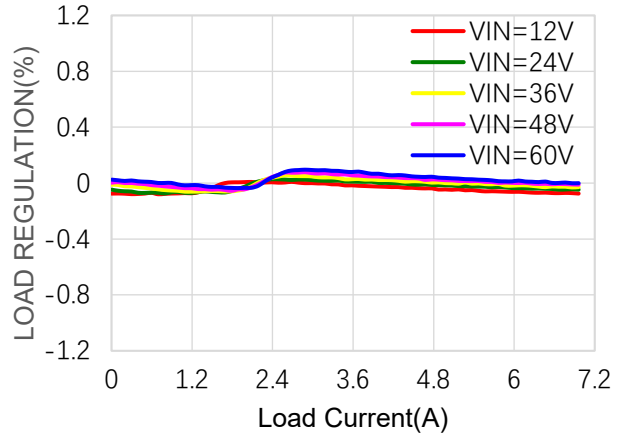


Figure 28. Load Regulation at 25°C

FUNCTION DESCRIPTION

General Description

The VE8600 is a high-performance, step-down, synchronous, DC/DC controller IC with a wide input voltage range. It implements current mode control and an internal slope compensation to avoid the subharmonic oscillation.

Diode Emulation Mode

The VE8600 offers diode emulation mode (DEM) functionality to optimize efficiency during light load. DEM is enabled when CCM/DEM is at a low level by connecting an appropriate resistor ($R_{CCM/DEM}$) to SGND.

The recommended value for $R_{CCM/DEM}$ is

$$0.5R_{FREQ} < R_{CCM/DEM} < 1.5R_{FREQ}$$

The value less than $0.5R_{FREQ}$ is not allowed but the value higher than $1.5R_{FREQ}$ and less than $3R_{FREQ}$ is allowed. The higher value of $R_{CCM/DEM}$ increases output voltage ripple but reduces the power loss during light load.

Gate Driver

The low-side gate driver is supplied from VCC. The high-side gate driver is supplied from BST. A boot capacitor connected from the BST to the VCC provides power to the high-side MOSFET driver. This floating driver has its own under-voltage lockout (UVLO) protection. This UVLO's rising threshold is 3.6V with a hysteresis of 100mV. If the BST voltage is lower than the bootstrap UVLO, the VE8600 enters boot refresh mode to ensure that the BST capacitor is high enough to drive the HS-FET.

Error Amplifier

The error amplifier compares V_{FB} with the internal 0.8V reference and outputs a current proportional to the difference between the two input voltages. This output current is then used to charge or discharge the external compensation network to form V_{COMP}, which is used to control the inductor current. Adjusting the compensation network from COMP to SGND optimizes the control loop for good stability or fast transient response.

Current Limit Function

There are three fixed current limit options: 23mV, when ILIM is connected to SGND; 48mV, when ILIM is connected to VCC; and 74mV, when ILIM is floating.

When the peak value of the inductor current exceeds the set current-limit threshold, the output voltage begins dropping until FB is 37.5% below the reference. The VE8600 enters hiccup mode to restart the part periodically. All switchers are turned off for 28ms before a re-start up is issued. The frequency is lowered when FB is below 0.4V. This protection mode is especially useful when the output is dead shorted to ground. The average short circuit current is reduced greatly to alleviate thermal issues. The VE8600 exits hiccup mode once the over-current condition is removed.

The VE8600 works on peak valley current limit mode and the hiccup mode is disabled when the voltage on the ILIM is between 0.64V and 1.5V before soft start. The current limit threshold can be calculated by Equation(1):

$$I_{LIM} = \frac{V_{ILIM} - 0.64}{10 \times R_S} \quad (1)$$

Low Dropout Mode

In low dropout mode, the VE8600 is designed to operate in low frequency mode as long as the off time is min-off time, improving dropout, increasing the effective duty cycle of the switching regulator. Low dropout operation makes the VE8600 suitable for automotive cold-crank applications.

Power Good

The VE8600 includes an open-drain power good output that indicates whether the regulator's output is within ±10% of its nominal value. When the output voltage falls outside of this range, the PG output is pulled low. PG should be connected to a voltage source no more than 5V through a resistor (e.g.: 100kΩ).

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V to 2.8V. When it is lower than REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

An external capacitor connected from SS to SGND is charged from an internal 4μA current source, producing a ramped voltage. The soft- start time (T_{SS}) is set by the external SS capacitor and can be calculated by Equation (2):

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(uA)} \quad (2)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.8V), and I_{SS} is the 4μA SS charge current. There is no internal SS capacitor. SS is reset when a fault protection other than OVP or peak valley current limit occurs.

Programmable Switching Frequency

The VE8600's frequency can be programmed from 100kHz to 1000kHz with a resistor from FREQ to SGND. The Value of R_{FREQ} can be calculated with Equation (3):

$$R_{FREQ}(K\Omega) = \frac{1000}{0.0202 \times F_{SW}(KHz)} - 9 \quad (3)$$

OVP

The output over-voltage is monitored by V_{FB}. If V_{FB} is typically 16% higher than the reference, the VE8600 enters discharge mode. The HS-FET turn off, and the LS-FET turns on. The LS-FET remains on until the reverse current limit is triggered. The LS-FET then turns off, and the inductor current increases to 0. The LS-FET is turned on again after ZCD is triggered. The VE8600 works in discharge mode until the over-voltage condition is cleared.

EN/SYNC

The VE8600 has a dedicated enable (EN/SYNC) control that uses a bandgap- generated precision threshold of 1.2V. By pulling EN/SYNC high or low, the IC can be enabled or disabled. To disable the part, EN/SYNC must be pulled low for at least 42μs. The device can be synchronized to an external clock ranging from 100kHz up to 1000kHz through EN/SYNC. The internal clock rising edge is synchronized to the external clock rising edge. The pulse width (both high and low) of the external clock signal should be no less than 100ns. The frequency applied on EN/SYNC pin of external clock must be higher than the frequency set by the FREQ pin.

SYNCO Function

The SYNCO pin outputs a default 180º phase shifted clock when VE8600 works in CCM. This function allows two devices operate in same frequency but 180°out of phase to reduce the total input current ripple. The SYCNO outputs a high level when VE8600 works on skip mode. The SYNCO pin outputs a default 180º phase shifted clock when it is synchronized by external clock.

Dithering Function

If VE8600 is set to CCM. It works on dithering mode when the SYNCO pin is shorted to GND before start up.

UVLO

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at an insufficient input supply voltage. The VE8600 UVLO rising threshold is about 4.1V, while its falling threshold is a consistent 3.8V.

Thermal Protection

Thermal protection prevents damage to the IC from excessive temperature. The die temperature is monitored internally until the thermal limit is reached. When the silicon die temperature is higher than 170°C, the entire chip shuts down. When the temperature is lower than its lower threshold (typically 150°C), the chip is enabled again.

Start-Up and Shutdown

If both V_{IN} and EN/SYNC are higher than their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents. The internal regulator is then enabled. The regulator provides a stable supply for the remaining circuitry. Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signal path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down.

Pre-Bias Start-Up

If SS is less than FB at start-up, and the output has a pre-bias voltage, neither TG nor BG is turned on until SS is greater than FB.

VCC Regulator Connection

VCC can be powered from both VIN and EXTBIAS. If connecting EXTBIAS to an external power supply to improve the overall efficiency, EXTBIAS should be higher than 5V but less than 24V. If V_{OUT} is higher than 4.7V but less than 24V, EXTBIAS can be connected to V_{OUT} with a resistor or diode. The recommend value of this resistor is 10Ω.

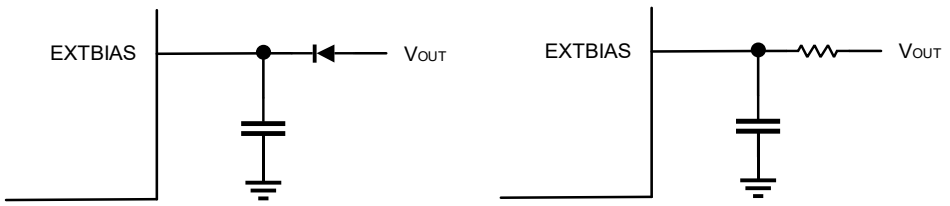


Figure 29. VCC Regulator Connection

APPLICATION

Setting the output voltage

The external resistor divider is used to set the output voltage (see Figure 30.).

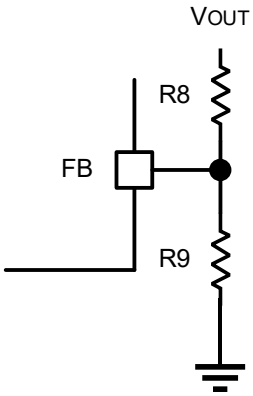


Figure 30. Setting the Output Voltage

If R8 is known, then R9 can be calculated with Equation (4):

$$R9 = R8 \div \left(\frac{V_{OUT}}{0.8V} - 1\right) \quad (4)$$

Setting Current Limit

The VE8600 has three fixed current limit options: 23mV (V_{SENSE+} - V_{SENSE-}), when ILIM is connected to SGND; 48mV, when ILIM is connected to VCC; and 74mV, when ILIM is floating. Ensure that the application can deliver a full load of current over the full operating temperature range when setting ILIM.

The current sense resistor (R_{SENSE}) monitors the inductor current. Its value is chosen based on the current limit threshold. The relationship between the peak inductor current (I_{PK}) and R_{SENSE} can be calculated with Equation (5):

$$R_{SENSE} = \frac{V_{ILIMIT}}{I_{PK}} \quad (5)$$

The VE8600 works on peak valley current limit mode and the hiccup mode is disabled when the voltage on the ILIM is between 0.64V and 1.5V before soft start. The current limit threshold can be calculated by Equation (1). The VE8600 integrates a 5uA current source and a 500kΩ resistor. The Voltage on the ILIM pin is 2.5V when this pin is floating.

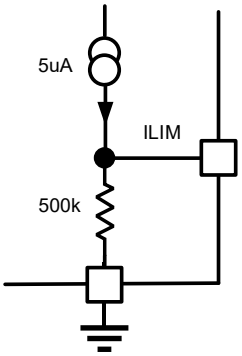


Figure 31. ILIM Internal Circuit

Slope compensation

An internal slope compensation is designed to avoid the subharmonic issue. The value of this slope is 400mV when the duty cycle is maximum. To avoid the subharmonic issue the inductor L can be calculated with Equation (6):

$$L > \frac{V_{OUT} \times 12 \times R_{SENSE}}{0.8 \times Fsw} \qquad (6)$$

where F_{SW} is the switching frequency.

BST Charge Diode and Resistor Selection

The recommended external BST diode is a Schottky diode. The recommended BST capacitor value is 0.1μF to 1μF and it must be less than 1/10 C_{VCC}. A resistor in series with the BST capacitor (R_{BST}) can reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce voltage stress at a high V_{IN}. A higher resistance is better for SW spike reduction but compromises efficiency. To make a tradeoff between EMI and efficiency, a ≤ 20Ω R_{BST} is recommended.

DCR sensing

For the applications requiring low cost with low power loss, DCR is used to sense the inductor current rather than using a sense resistor. Shown in Figure 32. is a DCR sensing configuration.

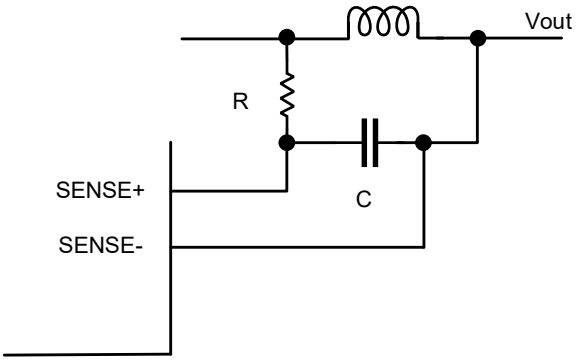


Figure 32. DCR sensing configuration

R and C selection should meet Equation (7) since this indirect current sensing method requires a time constant matching. R is usually selected to be in the range of 1kΩ to10kΩ and C can be calculated with Equation (7):

$$C = \frac{L}{DCR \times R} \qquad (7)$$

Switching frequency

Switching frequency selection is a trade-off between efficiency and component size. Low switching frequency improves efficiency by reducing MOSFET switching loss. To meet the output ripple and load transient requirements, operation at a low switching frequency requires larger inductance and output capacitance. The switching frequency of the VE8600 is set by a resistor connected from the FREQ pin to GND according to Equation (3). In noise-sensitive applications, the switching frequency should be out of a sensitive frequency band.

Selecting the Inductor

An inductor with a DC current rating at least 20% higher than the maximum load current is recommended for most applications. A larger value inductor results in less ripple current and a lower output ripple voltage. However, the larger value inductor has a larger size, higher series resistance, and lower saturation current. Choose the inductor ripple current to be approximately 20%~50% of the maximum load current. The inductance values can be calculated with Equation (8):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{SW}} \qquad (8)$$

Selecting the Output Capacitor

The output capacitor is used to hold output voltage and suppress the output voltage ripple. The output voltage ripple can be estimated with Equation (9):

$$V_{RIPPLE} = \frac{V_{OUT}}{L \times F_{SW}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\left(R_{ESR} + \frac{1}{8F_{SW} \times C_O}\right) \qquad (9)$$

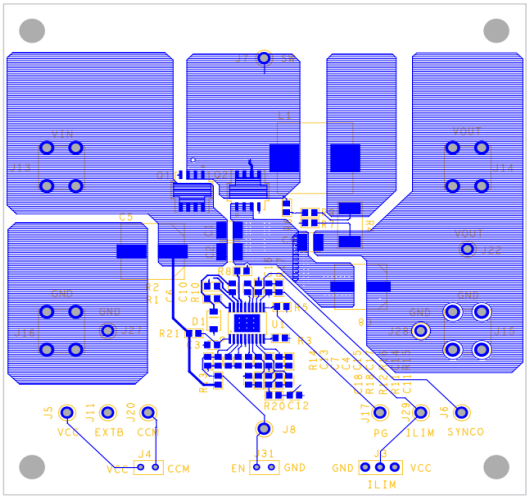
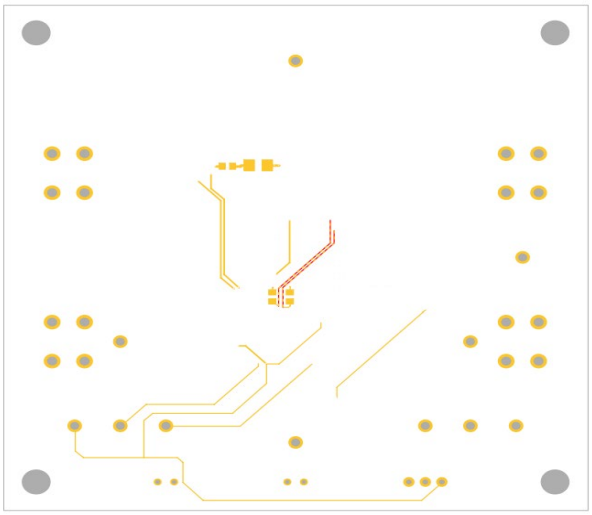
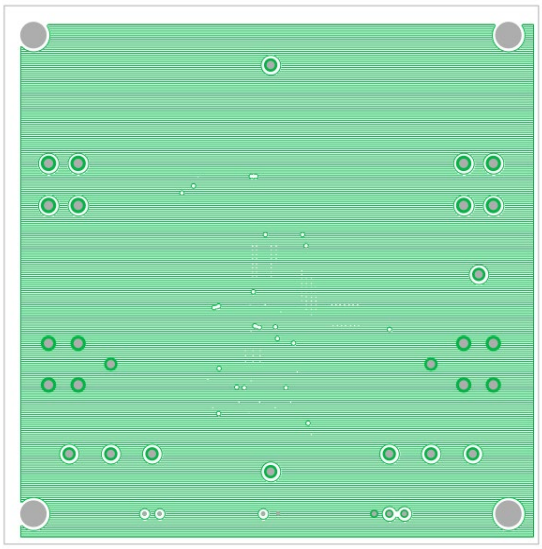
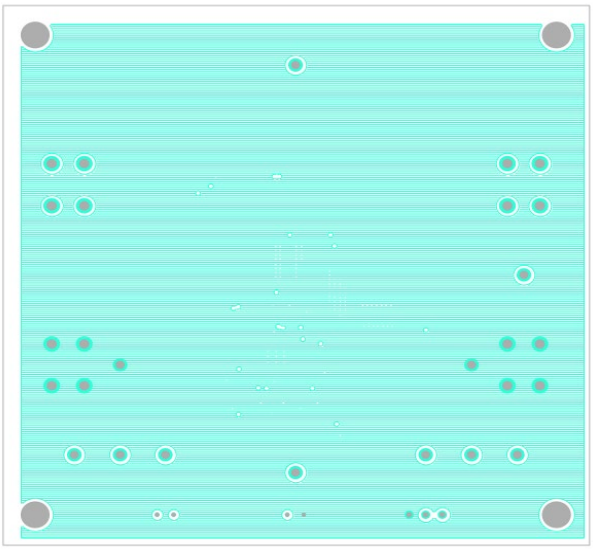
Power MOSFET Selection

Two N-channel MOSFETs must be selected for the controller: one for the high-side switch, and one for the low-side switch. The driver level of the high-side and low-side MOSFETs is 5V, the logic level MOSFET is recommend.

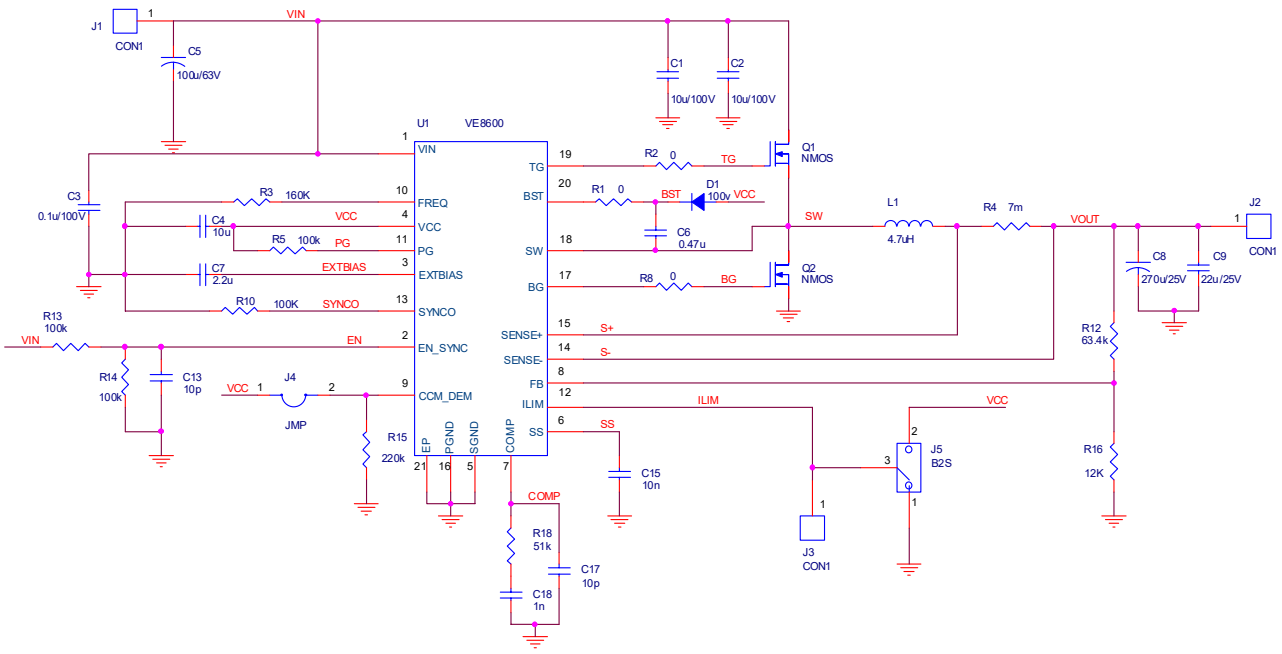
PCB Layout Guidelines

Efficient PCB layout is critical to achieve good regulation, ripple rejection, transient response, and thermal performance. It is highly recommended to duplicate the EVB layout for optimum performance. If changes are necessary, refer to below figures and follow the guidelines below:

1. A four-layer layout is strongly recommended to achieve better thermal performance.
2. Place input bypass ceramic capacitors close to VIN pin. Place the MOSFETs as close as possible to the device.
3. Place the feedback resistors close to the chip to ensure that the trace which connects to FB is as short as possible. Route SW and BST away from sensitive analog areas such as FB, SENSE+ and SENSE -.
4. Use a large ground plane to connect to PGND directly. Add vias near PGND if the bottom layer is a ground plane. Use multiple vias to connect the power planes to the internal layers.
5. Ensure the high-current paths at PGND and VIN have short, direct, and wide traces.
6. SENSE+ and SENSE - are differential pair, make the sense lines run close together, require close parallel and equal length routing. The purpose is to reduce the line drop error.

Top Layer	Bottom Layer
	
Inner layer 1	**Inner layer 2**
	

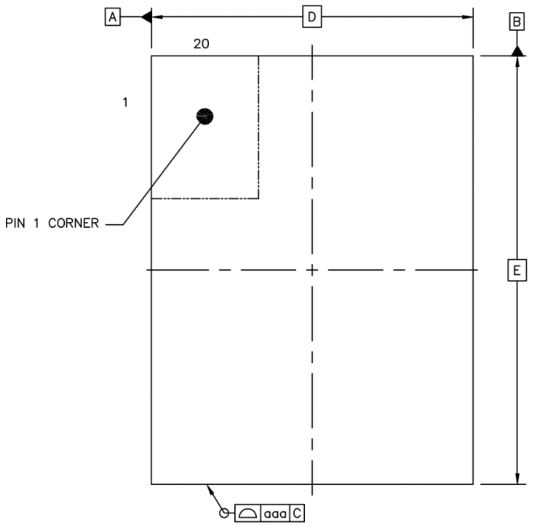
TYPICAL APPLICATION CIRCUITS



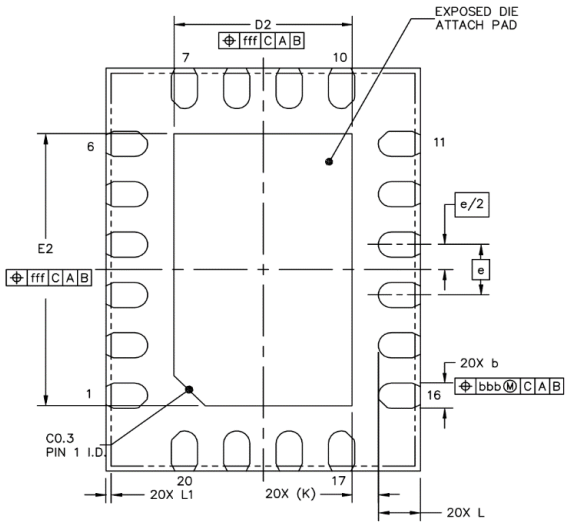
V_{IN} = 6-60V, V_{OUT} = 5V， I_{OUT} = 7A application

PACKAGE INFORMATION

QFN3x4-20 (Wettable Flank)

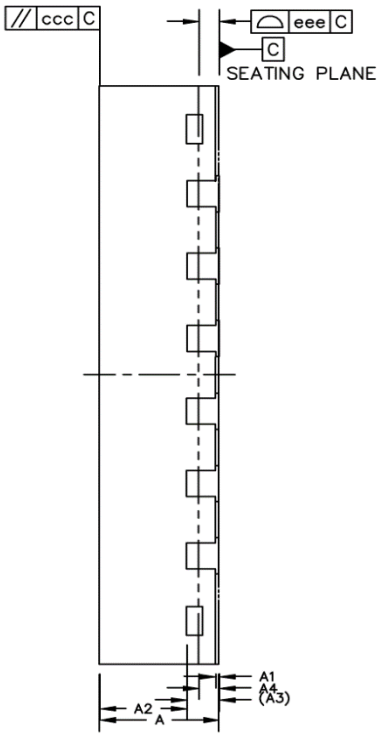


TOP VIEW



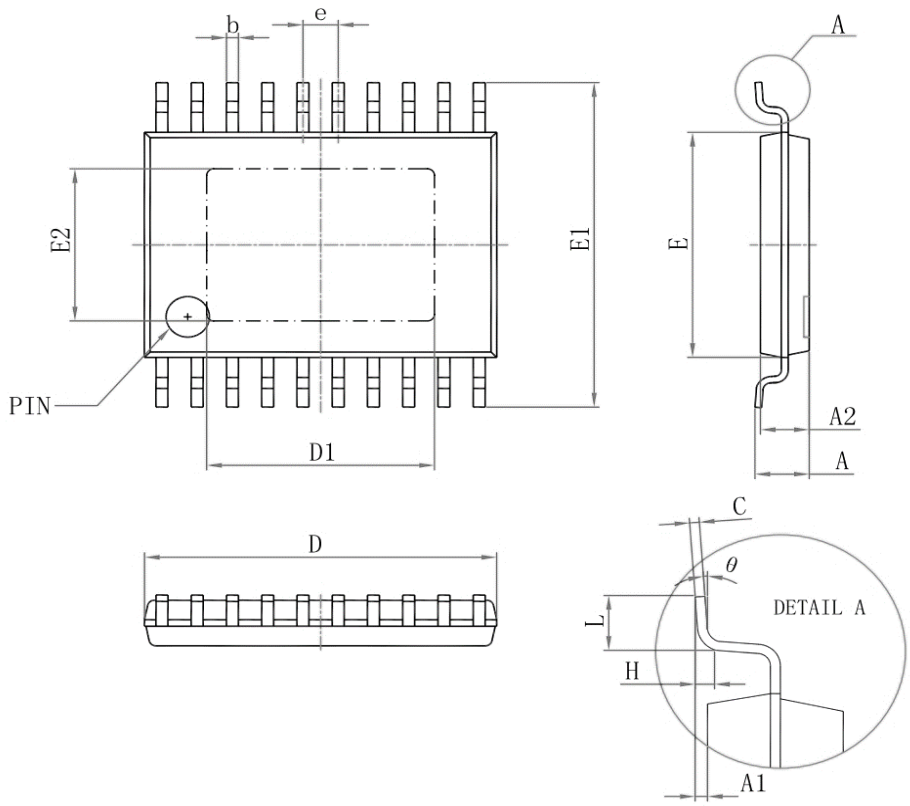
BOTTOM VIEW

Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.8	0.028	0.030	0.031
A1	——	0.02	0.05	——	0.001	0.002
A2	——	0.55	——	——	0.022	——
A3	0.203REF			0.008REF		
A4	0.075		0.18	0.003		0.007
b	0.2	0.25	0.3	0.008	0.010	0.012
D	3BSC			0.118 BSC		
E	4BSC			0.157 BSC		
e	0.5BSC			0.020BSC		
L	0.3	0.4	0.5	0.012	0.016	0.020
D2	1.6	1.7	1.8	0.063	0.067	0.071
E2	2.6	2.7	2.8	0.102	0.106	0.110
L1	0.01		0.09	0.0004		0.0035
K	0.25REF			0.0098 REF		
aaa	0.1			0.004		
bbb	0.1			0.004		
ccc	0.1			0.004		
eee	0.08			0.003		
fff	0.1			0.004		



SIDE VIEW

TSSOP20-EP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	6.4	6.6	0.252	0.259
D1	4.1	4.3	0.165	0.169
E	4.3	4.5	0.169	0.177
b	0.19	0.3	0.007	0.012
c	0.09	0.2	0.004	0.008
E1	6.25	6.55	0.246	0.258
E2	2.9	3.1	0.114	0.122
A		1.1		0.043
A2	0.8	1.0	0.031	0.039
A1	0.02	0.15	0.001	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.5	0.7	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

REVISION HISTORY

Revision	Data	Description
1.0	2024-05-06	Initial Release