Dual Channel 20V 6A Synchronous Step-Down Regulator

DESCRIPTION

The VE2266 is a high efficiency, dual-channel monolithic synchronous buck regulator using a controlled on-time current mode architecture, with phase lockable switching frequency. The operating supply voltage range is from 3.3V to 20V, making it suitable for lithium-ion battery stacks as well as point of load power supply applications from a 12V or 5V input.

The operating frequency is programmable from 500kHz to 4MHz with an external resistor and may be synchronized to an external clock signal. The high frequency capability allows the use of small surface mount inductors and capacitors. The unique constant frequency/controlled on- time architecture is ideal for high step-down ratio applications that operate at high frequency while demanding fast transient response.

The VE2266 can select between forced continuous mode and high efficiency Burst Mode operation. The VE2266 and VE2266A differ in their output voltage sense range.

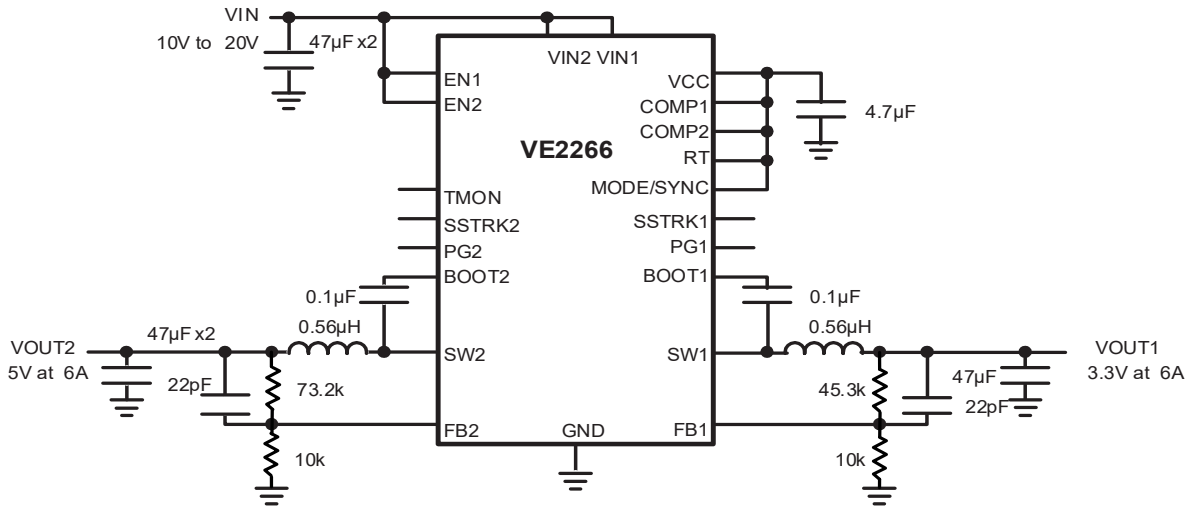
FEATURES

- Wide V_{IN} Range: 3.3 V to 20V
- Wide V_{OUT} Range:
  - 0.6V to 5V(VE2266)
  - 1.8V to 12V(VE2266A)
- Output Current per Channel: 6A
- High Efficiency: Up to 95%
- Die Temperature Monitor
- Adjustable Frequency: 500kHz to 4MHz
- External Frequency Synchronization
- Current Mode Operation for Excellent Line and Load Transient Response
- 0.6V Reference Allows Low Output Voltages
- User Selectable Burst Mode Operation or Forced Continuous Operation
- Output Voltage Tracking and Soft-Start Capability
- Short-Circuit Protected
- Overvoltage Input and Overtemperature Protection
- Power Good Status Outputs
- Low Profile 4mm × 5mm 28-Lead QFN Package

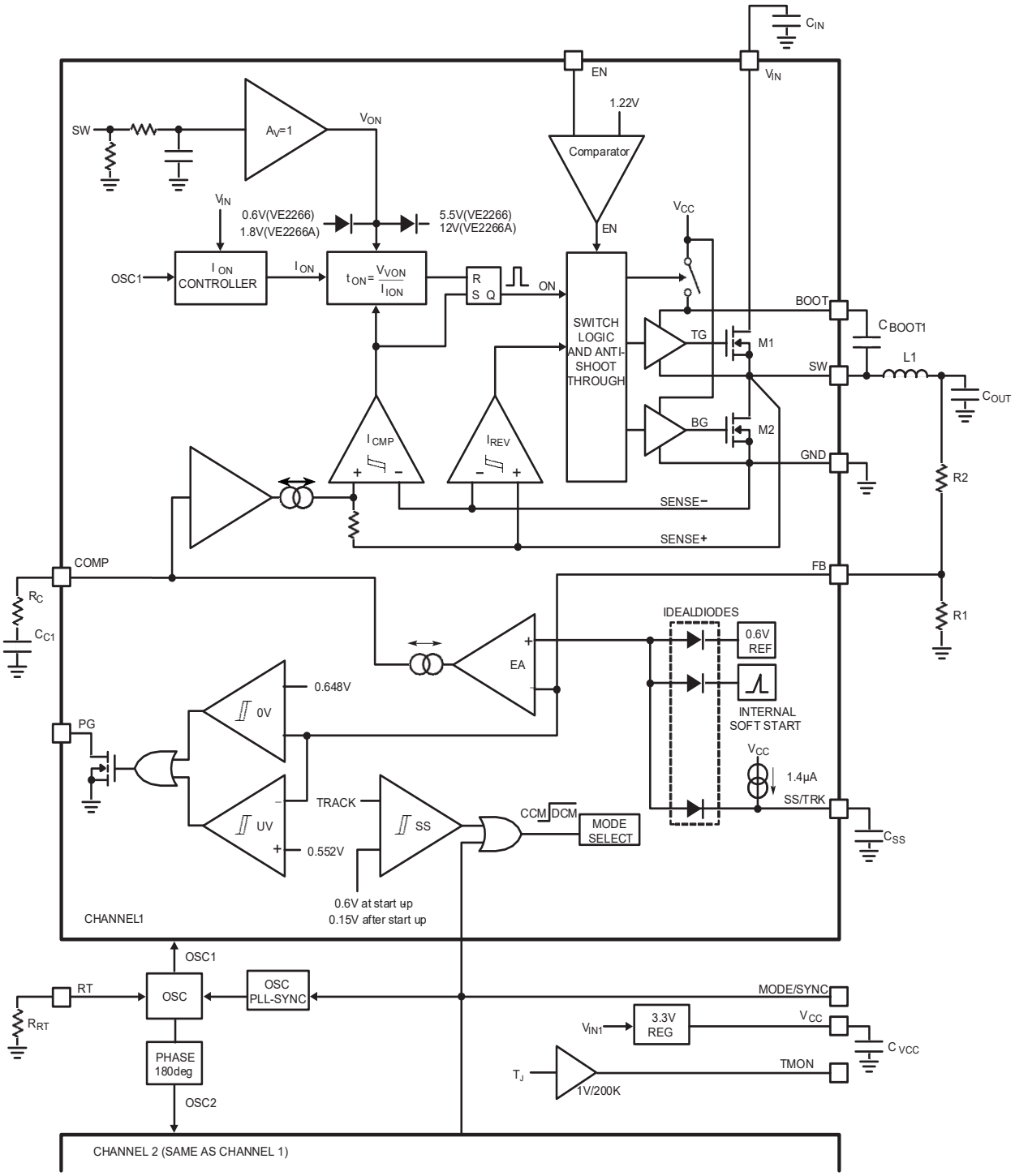
APPLICATIONS

- Industrial systems

TYPICAL APPLICATION



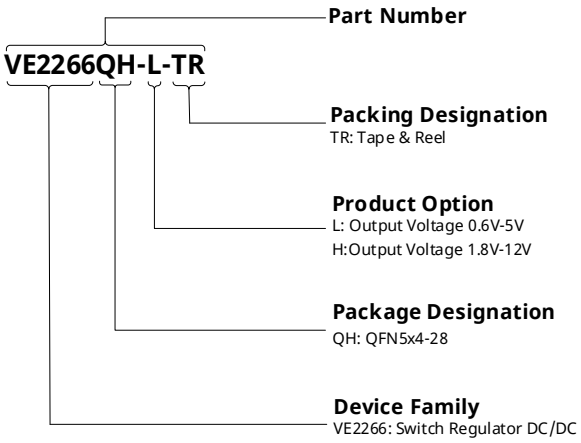
BLOCK DIAGRAM



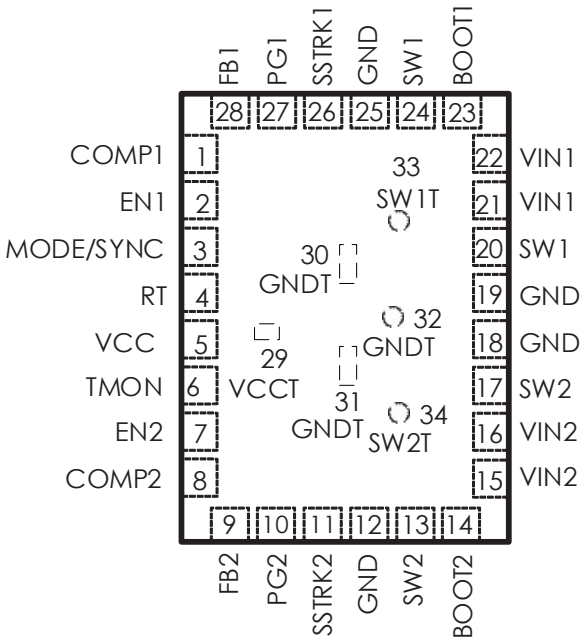
ORDERING INFORMATION

Ordering Information	Mark	Option	Temperature Range	Package	Pack	Quantity
VE2266QH-L-TR	2266L	L	-40 to +125°C	QFN4x5-28	TR	5000
VE2266QH-H-TR	2266H	H	-40 to +125°C	QFN4x5-28	TR	5000
VE2266P(1)			-40 to +125°C			

Note 1: This product is available only in wafer form and is not offered in packaged versions.



PIN CONFIGURATIONS



28-LEAD(4mmx5mm) PLASTIC QFN

PIN DESCRIPTION

PIN Name	QFN4X5-28	Description
COMP1	1	**Channel 1 Error Amplifier Output and Switching Regulator Compensation Point.** Connect this pin to appropriate external components to compensate the regulator loop frequency response.
EN1	2	**Channel 1 Regulator Enable Pin.** Enables channel 1 operation by tying EN above 1.25V. Tying it below 1V places the part into shutdown. Do not float this pin.
MODE/SYNC	3	**Mode Select and External Synchronization Input.** Tie this pin to ground to force continuous synchronous operation. Floating this pin or tying it to V_{CC} enables high efficiency Burst Mode operation at light loads. Drive this pin with a clock to synchronize the VE2266/VE2266A switching frequency. An internal phase-locked loop will force the bottom power NMOS's turn on signal to be synchronized with the rising edge of the CLKIN signal. When this pin is driven with a clock, forced continuous mode is automatically selected.
RT	4	**Oscillator Frequency Program Pin.** Connect an external resistor (between 80k to 640k) from this pin to GND in order to program the frequency from 500kHz to 4MHz. When RT is tied to V_{CC}, the switching frequency will default

PIN Name	QFN4X5-28	Description
		to 2MHz.
VCC	5	**Internal 3.3V Regulator Output.** The internal power drivers and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7μF low ESR ceramic capacitor.
TMON	6	**Temperature Monitor Output.** A voltage proportional to the measured on-die temperature will appear at this pin. The voltage-to-temperature scaling factor is 200°K/V. See the Applications Information section for detailed information on the TMON function. Tie this pin to V_{CC} to disable the temperature monitor circuit.
EN2	7	**Channel 2 Regulator Enable Pin.** Enables channel 2 operation by tying EN above 1.22V. Tying it below 1V places the part into shutdown. Do not float this pin.
COMP2	8	**Channel 2 Error Amplifier Output and Switching Regulator Compensation Pin.** Connect this pin to appropriate external components to compensate the regulator loop frequency response.
FB2	9	**Channel 2 Output Feedback Voltage Pin.** Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. Connect this pin to a resistor divider network to program the desired output voltage.
PG2	10	**Channel 2 Open-Drain Power Good Output Pin.** PG2 is pulled to ground when the voltage on the FB2 pin is not within ±8% (typical) of the internal 0.6V reference. PG2 becomes high impedance once the FB2 pin returns to within ±5% (typical) of the internal reference.
SSTRK2	11	**Soft-Start and Output Tracking Input Pin for Channel 2.** Forcing a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier. The VE2266/VE2266A will servo the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. An internal 1.4μA pull up current from V_{CC} allows a soft-start function to be implemented by connecting a capacitor between this pin and PGND.
GND	12,18,19,25	**Power and Signal Ground.** These pins must be tied together and soldered to PCB ground.
SW2	13,17	**Channel 2 Switch Node.** Connecting this pin to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to V_{IN}.
BOOT2	14	**Boot Floating Driver supply for Channel 2.** The (+) terminal of the bootstrap capacitor connects to this pin while the (–) terminal connects to the SW pin. The normal operational voltage swing of this pin ranges from a diode voltage drop below V_{CC} up to $V_{IN}+V_{CC}$.
VIN2	15,16	**Power Supply Input for Channel 2.** This input is capable of operating from a separate supply voltage than V_{IN1}.
SW1	20,24	**Channel 1 Switch Node.** Connecting this pin to External Inductor. Voltage

PIN Name	QFN4X5-28	Description
		swing of SW is from a diode voltage drop below ground to V_{IN}.
VIN1	21,22	**Power Supply Input for Channel 1.** Input voltage to the on chip power MOSFETs on channel 1. The internal LDO for V_{CC} is powered off of this pin.
BOOT1	23	**Boot Floating Driver supply for Channel 1.** The (+) terminal of the bootstrap capacitor connects to this pin while the (–) terminal connects to the SW pin. The normal operational voltage swing of this pin ranges from a diode voltage drop below V_{CC} up to V_{IN}+V_{CC}.
SSTRK1	26	**Soft-Start and Output Tracking Input Pin for Channel 1.** Forcing a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier. The VE2266/VE2266A will servo the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. An internal 1.4μA pull up current from V_{CC} allows a soft-start function to be implemented by connecting a capacitor between this pin and PGND.
PG1	27	**Channel 1 Open-Drain Power Good Output Pin**. PG1 is pulled to ground when the voltage on the FB1 pin is not within ±8% (typical) of the internal 0.6V reference. PG1 becomes high impedance once the FB1 pin returns to within ±5% (typical) of the internal reference.
FB1	28	**Channel 1 Output Feedback Voltage Pin.** Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. Connect this pin to a resistor divider network to program the desired output voltage.
VCCT	29	**Additional V_{CC} pin.** Not required to be connected to V_{CC} pin for operation.
GNDT	30,31,32	**Power Ground.** Additional power ground pins for improved thermal dissipation when connected to the GND pins. Not required to be connected to GND pins for operation.
SWT1T	33	**Additional SW1 pin.** Not required to be connected to SW1 pins 20 and 24 for operation.
SWT2T	34	**Additional SW2 pin.** Not required to be connected to SW2 pins 13 and 17 for operation.

ABSOLUTE MAXIMUM RATINGS

Parameter	Minimum	Maximum	Units
VIN1, VIN2	-0.3	22	V
PGOOD1, PGOOD2	-0.3	22	V
BOOT1-SW1, BOOT2-SW2	-0.3	3.6	V
SSTRK1, SSTRK2	-0.3	3.6	V
COMP1, COMP2, RT, MODE/SYNC	-0.3	V_{CC}+0.3	V
VFB1, VFB2, TMON	-0.3	V_{CC}+0.3	V
EN1, EN2	-0.3	22	V
Storage Temperature	-65	+150	°C
Maximum Reflow (Package Body) Temperature		260	°C

ESD RATINGS

Parameter	Value	Units
Human Body Model (HBM)	±1500	kV
Charged-device model (CDM)	±1250	V

THERMAL INFORMATION

Thermal Resistance	θ_{JA}(°C/W)	θ_{JC}(°C/W)
QFN4X5-28	21	7

RECOMMENDED OPERATINIG CONDITIONS

Parameter		Minimum	Maximum	Units
V_{IN}		3.3	20	V
V_{OUT}	VE2266	0.6	5.	V
	VE2266A	1.8	12	V
Operating Junction Temperature		-40	+125	°C

ECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Supply Range			●	3.3		20	V
V_{IN1} Supply Range			●	3.3		20	V
V_{IN2} Supply Range		3.3V<V_{IN1}<20V	●	1.5		20	V
Output Voltage Range (Note 4)	V_{OUT}	VE2266		0.6		5.5	V
		VE2266A		1.8		12	V
Input DC Supply Current (V_{IN1} + V_{IN2})	I_Q	Both Channels Active (Note 5) V_{FB1}, V_{FB2}>0.6			2.05		mA
		Shutdown V_{EN} = 0V			17		μA
Feedback Reference Voltage	V_{FB}		●		0.600		V
Feedback Voltage Line Regulation	ΔV_{LINE_REG}	V_{IN} = 3.3V to 20V			0.004		%/V
Feedback Voltage Load Regulation	ΔV_{LOAD_REG}	COMP = 0.8V to 1.6V			0.05		%
Feedback Pin Input Current	I_{FB}			-30		30	nA
Error Amplifier Transconductance	g_m(EA)	COMP = 1.2V			1.6		ms
Minimum On-Time	$T_{ON(MIN)}$	VE2266 VE2266A			35 35		ns
Minimum Off-Time	$T_{OFF(MIN)}$				130		ns
Oscillator Frequency	f_{OSC}	RT=162k			2		MHz
Valley Switch Current Limit	I_{LIM}	COMP=1.8V			6.6		A
Negative Valley Switch Current Limit					-4.2		A
Top Switch On-Resistance	R_{TOP}				32		mΩ
Bottom Switch On-Resistance	R_{BOT}				18		mΩ
Switch Leakage Current	$I_{SW(LKG)}$	V_{IN} = 20V, V_{EN} = 0V				63	μA
Internal Temperature Monitor		T_A=25°C			1.5		V
Internal Temperature Monitor Slope (Note6)					200		°C/V
V_{IN} Overvoltage Lockout Threshold	V_{IN-OV}	V_{IN} Rising V_{IN} Falling			22.2 21.1		V V
V_{CC} Voltage		3.6V<V_{IN}<20V, 0mA Load			3.3		V
V_{CC} Load Regulation		0mA to 50mA Load, V_{IN}=4V to 20V			1.3		%

Parameters	Symbol	Condition		Min	Typ	Max	Units
V_{CC} Undervoltage Lockout Threshold		V_{CC} Rising, $V_{IN}=V_{CC}$ V_{CC} Falling, $V_{IN}=V_{CC}$			3.05 2.8		V V
EN Threshold Rising			●		1.22		V
EN Threshold Falling			●		1.01		V
EN Leakage Current					0.5		μA
PG Good-to-Bad Threshold		V_{FB} Rising V_{FB} Falling			8 -8		% %
PG Bad-to-Good Threshold		V_{FB} Rising V_{FB} Falling			-6 6		% %
PG Pull-Down Resistance	R_{PG}	10mA Load			50		Ω
Power Good Filter Time	t_{PG}				40		μs
Internal Soft-Start Time	t_{SS}	10%to90% Rise Time			900		μs
V_{FB} During Tracking		TRACKS = 0.3V			0.3		V
TRACKS Pull-Up Current	I_{SSTRK}				1.4		μA
MODE/SYNC Threshold Voltage	$V_{MODE/SYNC}$	MODE V_{IH} MODE V_{IL}		1		 0.4	V V
SYNC Threshold Voltage		SYNC V_{IH}		0.9			V
MODE/SYNC Input Current	I_{MODE}	MODE = 0 V MODE = V_{CC}			6	 100	μA nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The VE2266 is tested under pulsed load conditions such that $T_J \approx T_A$. The VE2266 is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Output voltages outside the specified range are not optimized for controlled on-time operation. Refer to the Applications Information section for further discussions related to the output voltage range.

Note 5: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 6: Guaranteed by design.

Note 7: Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

TYPICAL PERFORMANCE GRAPHS

T_J=25°C, V_{IN1}=V_{IN2}=12V, V_{OUT}=3.3V, F_{SW}=1MHz, L=0.68μH unless otherwise noted.

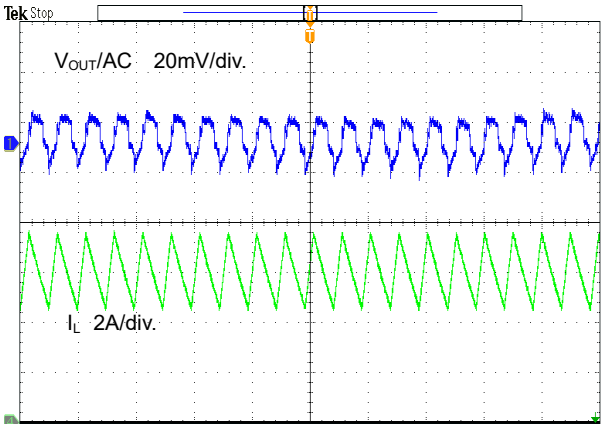


Figure 1. Load Transient 0A-6A

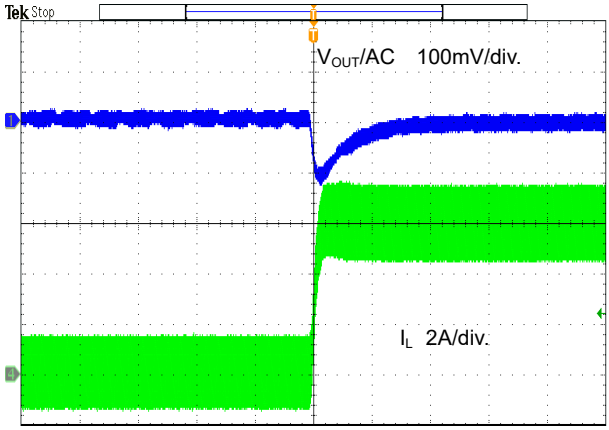


Figure 2. Load Transient 0A-6A

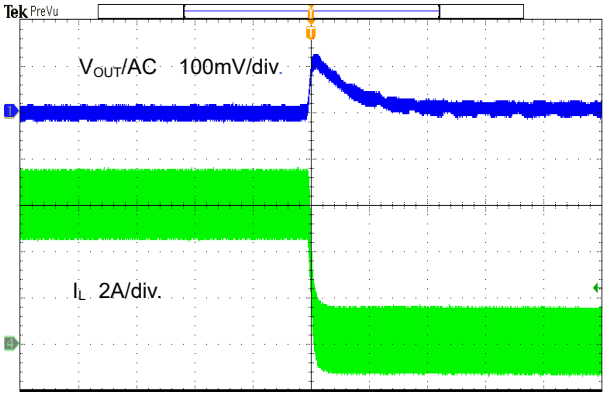


Figure 3. Load Transient 6A-0A

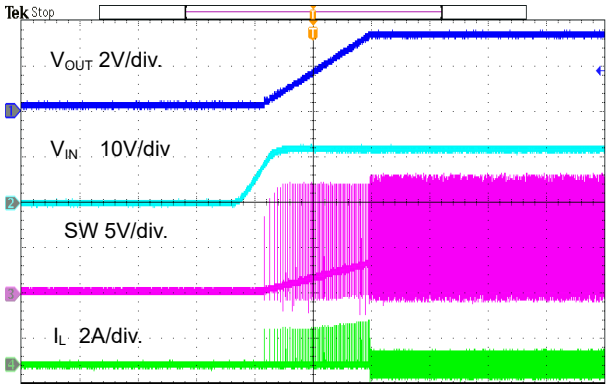


Figure 4. Vin Start-up No Load

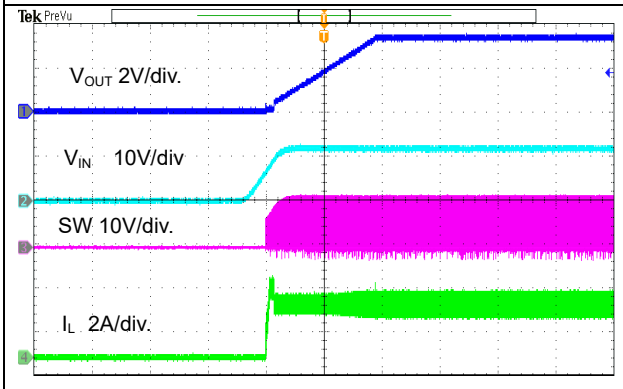


Figure 5. Vin Start-up Full Load

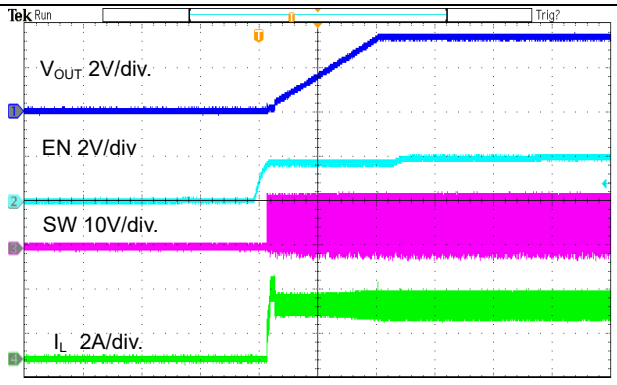


Figure 6. EN Start-up Full Load

TYPICAL PERFORMANCE GRAPHS

T_J=25°C, V_{IN1}=V_{IN2}=12V, V_{OUT}=3.3V, F_{SW}=1MHz, L=0.68μH unless otherwise noted.

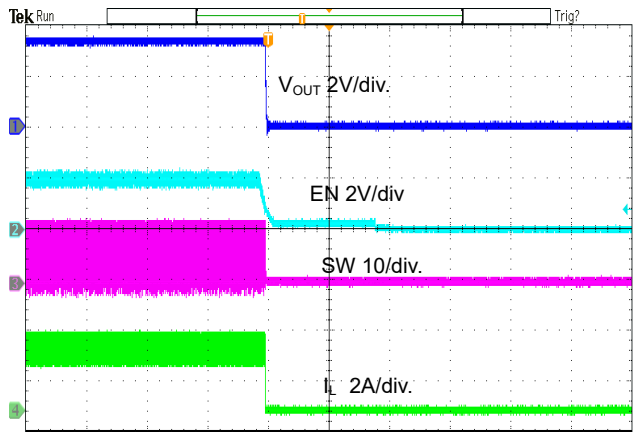


Figure 7. EN Shut-down Full Load

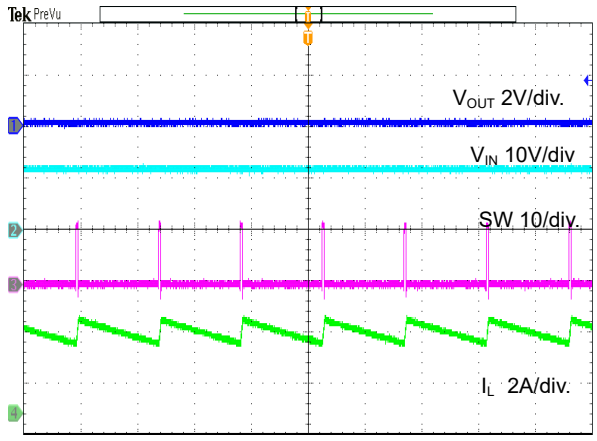


Figure 8. Short Circuit

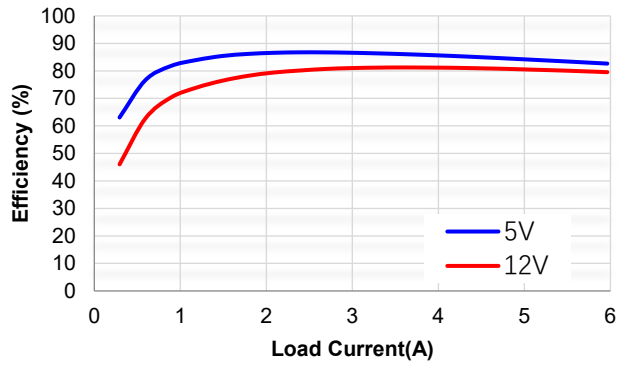


Figure 9. Efficiency-1.2Vout

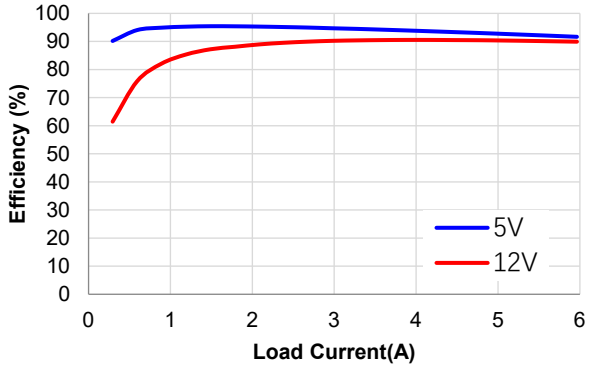


Figure 10. Efficiency-3.3Vout

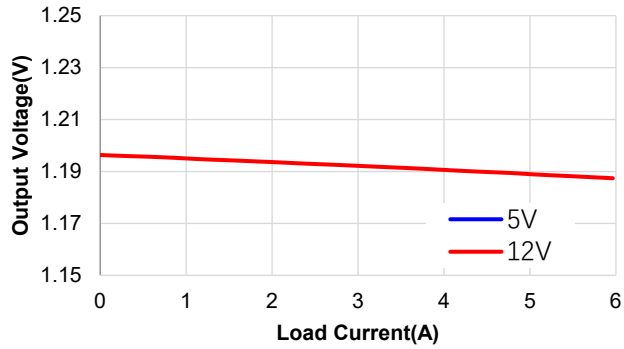


Figure 11. Load Regulation-1.2Vout

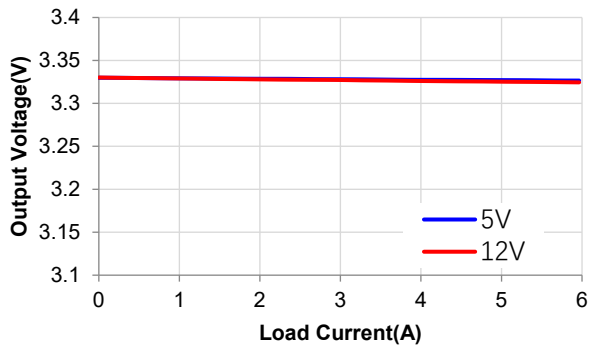


Figure 12. Load Regulation-3.3Vout

FUNCTION DESCRIPTION

General Description

The VE2266/VE2266A is a dual-channel, current mode monolithic step down regulator capable of providing 6A of output current from each channel. Its unique controlled on-time architecture allows extremely low step-down ratios while maintaining a constant switching frequency. Both channels share the same clock and run 180° out of phase. Each channel is enabled by raising the voltage on the EN pin above 1.22V nominally.

Main Control Loop

In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a fixed one-shot timer ("ON" signal in Block Diagram). When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator I_{CMP} trips, thus restarting the one shot timer and initiating the next cycle. Inductor current is measured by sensing the voltage drop across the SW and GND nodes of the bottom power MOSFET. The voltage on the COMP pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this COMP voltage by comparing an internal 0.6V reference to the feedback signal FB derived from the output voltage. If the load current increases, it causes a drop in the feedback voltage relative to the internal reference. The COMP voltage then rises until the average inductor current matches that of the load current.

The operating frequency is determined by the value of the RT resistor, which programs the current for the internal oscillator. An internal phase-locked loop servos the switching regulator on-time to track the internal oscillator edge and force a constant switching frequency. A clock signal can be applied to the MODE/SYNC pin to synchronize the switching frequency to an external source. The regulator defaults to forced continuous operation once the clock signal is applied.

At light load currents, the inductor current can drop to zero and become negative. In PFM mode operation, a current reversal comparator (IREV) detects the negative inductor current and shuts off the bottom power MOSFET, resulting in discontinuous operation and increased efficiency. Both power MOSFETs will remain off until the COMP voltage rises above the zero current level to initiate another cycle. During this time, the output capacitor supplies the load current and the part is placed into a low current sleep mode. Discontinuous mode operation is disabled by tying the MODE/SYNC pin to ground, which forces continuous synchronous operation regardless of output load current.

"Power Good" Status Output

The PG open-drain output will be pulled low if the regulator output exits a ±8% window around the regulation point. This condition is released once regulation within a ±5% window is achieved. To prevent unwanted PG glitches during transients or dynamic V_{OUT} changes, the VE2266/VE2266A PG falling edge includes a filter time of approximately 40μs.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient input voltage spikes, the VE2266/VE2266A constantly monitors each V_{IN} pin for an overvoltage condition. When V_{IN} rises above 22.1V, the regulator suspends operation by shutting off both power MOSFETs on the corresponding channel. Once V_{IN} drops below 21.1V, the regulator immediately resumes normal operation. The regulator executes its soft-start

function when exiting an overvoltage condition.

Overcurrent and Short-Circuit Protection

The VE2266 protects itself against output overcurrent and short-circuits by sensing the inductor valley current. When the current limit is reached, the output begins to fall, resulting in decreased on-time of the top power MOSFET. If the short is prolonged enough for the on-time to reach its minimum, the off-time will lengthen, lowering the switching frequency and preventing excess current from being drawn from V_{IN}. After the overcurrent or short is removed, the regulator executes its soft-start function to prevent the output voltage from overshooting. A general VE2266/VE2266A application circuit is shown on the first page of this data sheet. External component selection is largely driven by the load requirement and switching frequency. Component selection typically begins with the selection of the inductor L and resistor RT. Once the inductor is chosen, the input capacitor, C_{IN}, and the output capacitor, C_{OUT}, can be selected. Next, the feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as external loop compensation, soft-start/tracking, input UVLO, and PG.

Programming Switching Frequency

Selection of the switching frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

Connecting a resistor from the RT pin to GND programs the switching frequency (F_{SW}) between 500kHz and 4MHz according to the following formula:

$$R_{RT} = \frac{3.2 \times 10^{11}}{F_{SW}}$$

where RRT is in Ω and F_{SW} is in Hz.

When RT is tied to V_{CC}, the switching frequency will default to approximately 2MHz, as set by an internal resistor. This internal resistor is more sensitive to process and temperature variations than an external resistor (see

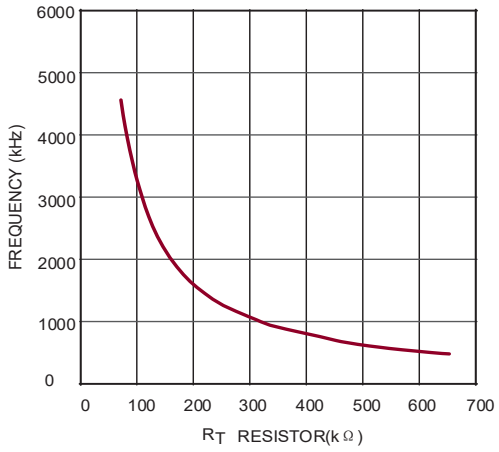


Figure 13 Switching Frequency vs RT

Typical Performance Characteristics) and is best used for applications where switching frequency accuracy is not critical.

Dual-Phase Single V_{OUT} Operation

For output loads that demand more than 6A of current, the two channels can be configured in parallel as a single output to provide more output current. During dual-phase operation, it is recommended to set the switching frequency above 800kHz to ensure stability over a wide input voltage range. With dual-phase operation, the two channels of the VE2266 are operated 180 degrees out of phase. This effectively interleaves the current pulses coming from the switches, greatly reducing the overlap time when they add together. The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used and reduces the voltage noise on the supply line.

The two channels in parallel will inherently share current well, because the VE2266 is a current mode controlled regulator. When operating the channels in parallel, tie the respective EN, SSTRK, FB, and COMP pins together; do not tie COMP pins to V_{CC}. Use external compensation on the combined COMP pins. Good current sharing balances the thermals on the design.

APPLICATION

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. More specifically, the inductor ripple current decreases with higher inductor value or higher operating frequency according to the following equation:

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \cdot L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where ΔI_L = inductor ripple current, f = operating frequency L = inductor value and V_{IN} is the input power supply voltage applied to the V_{IN} inputs. A trade-off between component size, efficiency and operating frequency can be seen from this equation. Accepting larger values of ΔI_L allows the use of lower value inductors but results in greater inductor core loss; greater ESR loss in the output capacitor; and larger output voltage ripple. Generally, highest efficiency operation is obtained at low operating frequency with small ripple current.

A reasonable starting point is to choose a ripple current of 2.4A which is about 40% of $I_{OUT(MAX)}$. Exceeding 60% of $I_{OUT(MAX)}$ is not recommended. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{F_{SW} \cdot \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire, leading to increased DCR and copper loss.

Ferrite designs exhibit very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current, so it is important to ensure that the core will not saturate.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements.

Table 1 gives a sampling of available surface mount inductors.

Table 1 Inductor Selection Table

Inductance (μH)	DCR (mΩ)	Max Current (A)	Dimensions (mm)	Height (mm)
Wurth WE-HC 744312 Series				
0.25	2.5	18	7x7.7	3.8
0.47	3.4	16		
0.72	7.5	12		
1.0	9.5	11		
1.5	10.5	9		
TDK SPM5030 Series				
0.22	2.31	21	5.2x5	3
0.35	4.29	14.9	5.2x5	3
TDK SPM6530 Series				
0.47	3.63	19.7	7.1x6.5	3
0.68	5.39	16.6		
1.0	7.81	13.2		
1.5	10.7	9.4		

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current is recommended. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS}=I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Even though the VE2266/VE2266A design includes an over-voltage protection circuit, care must always be taken to ensure input voltage transients do not pose an overvoltage hazard to the part.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is approximated by:

$$\Delta V_{OUT} < \Delta I_L \left(ESR + \frac{1}{8 \cdot F_{SW} \cdot C_{OUT}} \right)$$

When using low-ESR ceramic capacitors, it is more useful to choose the output capacitor value to fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support

the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor of approximately:

$$C_{OUT} \approx \frac{3 \cdot \Delta I_{OUT}}{F_{SW} \cdot V_{DROOP}}$$

Though this equation provides a good approximation, more capacitance may be required depending on the duty cycle and load step requirements. The actual V_{DROOP} should be verified by applying a load step to the output.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are available in small case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

V_{CC} Regulator Bypass Capacitor

An internal low dropout (LDO) regulator draws power from the V_{IN1} input and produces the 3.3V supply that powers the internal bias circuitry and drives the gate of the internal MOSFET switches. The V_{CC} pin connects to the output of this regulator and must have a minimum of 4.7μF ceramic decoupling capacitance to ground. The decoupling capacitor should have low impedance electrical connections to the V_{CC} and GND pins to provide the transient currents required by the VE2266/VE2266A. High input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Connecting any external load to the V_{CC} pin is not recommended since it may impact VE2266/VE2266A operation while increasing power dissipation and die temperature.

BOOT Capacitor

The VE2266/VE2266A uses a “bootstrap” circuit to create a voltage rail above the applied input voltage V_{IN}. Specifically, a boot capacitor, C_{BOOT}, is charged to a voltage approximately equal to V_{CC} each time the bottom power MOSFET is turned on. The charge on this capacitor is then used to supply the required transient current during the remainder of the switching cycle. When the top MOSFET is turned on, the BOOT pin voltage will be equal to approximately V_{IN} + 3.3V. For most applications, a 0.1μF ceramic capacitor closely connected between the BOOT and SW pins will provide adequate performance.

Output Voltage Programming

Each regulator’s output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.6V\left(1 + \frac{R2}{R1}\right)$$

The desired output voltage is set by appropriate selection of resistors R1 and R2 as shown in Figure 14. Choosing large values for R1 and R2 will result in improved zero-load efficiency but may lead to undesirable noise coupling or phase margin reduction due to stray capacitances at the FB node. Care should be taken to route the FB trace away from any noise source, such as the SW trace. To improve the frequency response of the main control loop, a feedforward capacitor, C_F, may be used as shown in Figure 14.

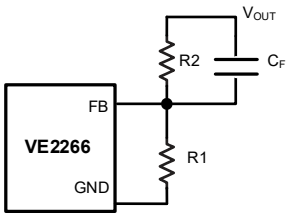


Figure 14. Setting the Output Voltage

If the output voltage is outside the V_{ON} sense range (0.6V – 5V for the VE2266, 1.8V–12V for the VE2266A), the output voltage will stay in regulation, but the switching frequency may deviate from the programmed frequency.

Minimum Off-Time/On-Time Considerations

The minimum off-time is the smallest amount of time that the VE2266/VE2266A can turn on the bottom power MOSFET, trip the current comparator and turn the power MOSFET back off. This time is typically 130ns. For the controlled on-time architecture, the minimum off-time limit imposes a maximum duty cycle of:

$$Duty_{MAX} = 1 - F_{SW} \cdot \left(T_{OFF(MIN)} + 2 \cdot T_{DEAD}\right)$$

where F_{SW} is the switching frequency, t_{DEAD} is the nonoverlap time, or “dead time” (typically 5ns) and $T_{OFF(MIN)}$ is the minimum off-time. If the maximum duty cycle is surpassed, due to a dropping input voltage for example, the output will drop out of regulation. The minimum input voltage to avoid this dropout condition is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{1 - F_{SW} \cdot \left(T_{OFF(MIN)} + 2 \cdot T_{DEAD}\right)}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its “on” state. This time is typically 35ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$Duty_{MIN} = F_{SW} \cdot T_{ON(MIN)}$$

where $T_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This constraint may not be of critical importance in most cases, so high switching frequencies may be used in the design without any fear of severe consequences. As the sections on Inductor and Capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the footprint of the application circuit.

External Loop Compensation

The VE2266/VE2266A provides the option to choose specific external loop compensation components to

optimize the main control loop transient response as desired. External loop compensation is chosen by simply connecting the desired network to the COMP pin.

Suggested compensation component values are shown in Figure 15. For a 2MHz application, an R-C network of 2.2nF and 20kΩ provides a good starting point. The bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. A 22pF bypass capacitor on the COMP pin is recommended for the purposes of filtering out high frequency coupling from stray board capacitance. In addition, a feedforward capacitor C_F can be added to improve the high frequency response, as previously shown in Figure 14. Capacitor C_F provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

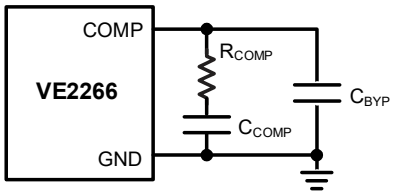


Figure 15. Compensation Component

Checking Transient Response

The regulator loop response can be checked by observing the response of the system to a load step. When configured for external compensation, the availability of the COMP pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC filtered closed loop response test point. The DC step, rise time, and settling behavior at this test point reflect the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The COMP external components shown in Figure 15. circuit will provide an adequate starting point for most applications. The series R-C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PCB layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of ~1μs will produce output voltage and COMP pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

When observing the response of V_{OUT} to a load step, the initial output voltage step may not be within the bandwidth of the feedback loop. In this case, the standard second order overshoot/DC ratio cannot be used to determine phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

In some applications, a more severe transient can be caused by switching in loads with large (>10μF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A hot swap

controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft starting.

On-Die Temperature Monitor

The VE2266/VE2266A produces a voltage at the TMON pin proportional to the measured junction temperature. The junction temperature-to-voltage scaling factor is 200K/V. Thus, to obtain the junction temperature in degrees Kelvin, simply multiply the voltage provided at the TMON pin by the scaling factor. To obtain the junction temperature in degrees Celsius, subtract 273 from the value obtained in degrees Kelvin.

The temperature monitor function uses a chopping technique to achieve high precision. As a result, a small periodic ripple may be seen at the TMON pin, the average of which is the measured value of interest. The ripple frequency will be the operating frequency divided by 32. If required, a 1μF or greater capacitor to GND may be placed on the output to reduce the magnitude of the ripple.

MODE/SYNC Operation

The MODE/SYNC pin is a multipurpose pin allowing both mode selection and operating frequency synchronization. Floating this pin or connecting it to V_{CC} enables PFM Mode operation for superior efficiency at low load currents at the expense of slightly higher output voltage ripple. When the MODE/SYNC pin is tied to ground, forced continuous mode operation is selected, creating the lowest fixed output ripple at the expense of light load efficiency.

The VE2266/VE2266A will detect the presence of the external clock signal on the MODE/SYNC pin and synchronize the internal oscillator to the phase and frequency of the incoming clock. The presence of an external clock will place both regulators into forced continuous mode operation. The internal PLL has a synchronization range of ±30% around its programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this ±30% range of the RT programmed frequency.

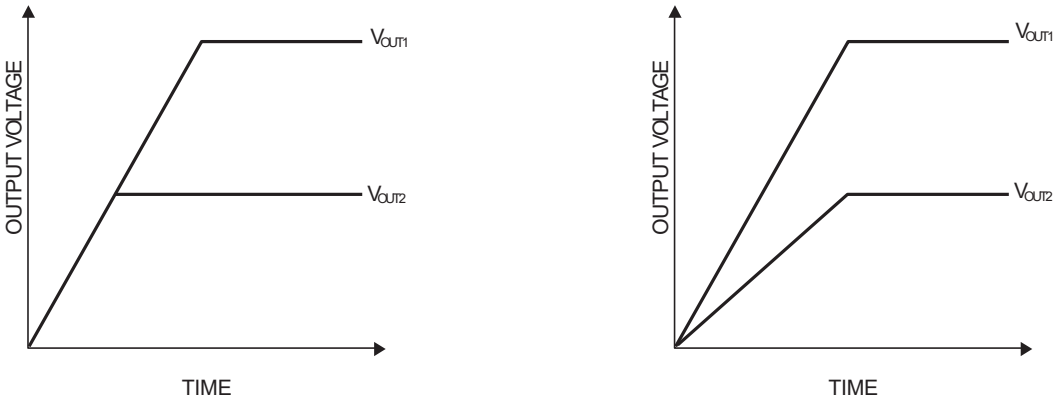
Output Voltage Soft-Start and Tracking

The VE2266/VE2266A allows the user to control the output voltage ramp rate by means of the SSTRK pin.

From 0 to 0.6V, the SSTRK voltage will override the internal 0.6V reference input to the error amplifier, thus regulating the feedback voltage to that of the SSTRK pin. When SSTRK is above 0.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

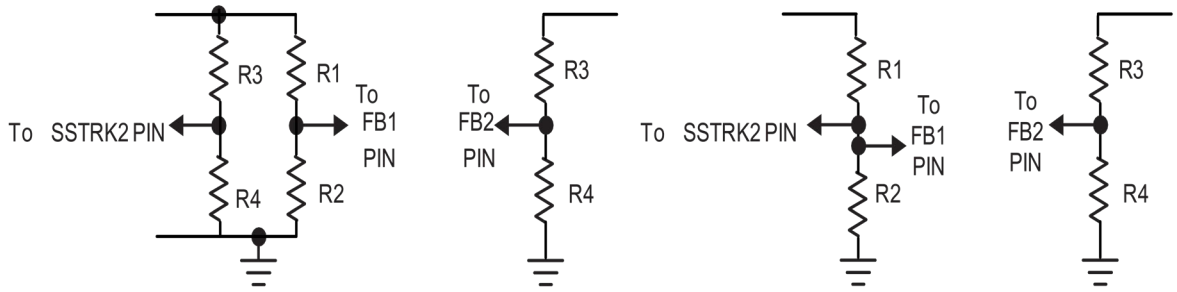
The voltage at the SSTRK pin may be driven from an external source, or alternatively, the user may leverage the internal 1.4μA pull-up current source to implement a soft-start function by connecting an external capacitor (C_{SS}) from the SSTRK pin to ground. The relationship between output rise time and SSTRK capacitance is given by:

$$T_{SS} = 430000\Omega \cdot C_{SS}$$



(a) Coincident Tracking (b) Ratiometric Tracking

Figure 16. Two Differential Modes of Output Voltage Tracking



(a) Coincident Tracking (b) Ratiometric Tracking

Figure 17. Setup for Coincident and Ratiometric Tracking

A default internal soft-start ramp forces a minimum soft- start time of 1000μs by overriding the SSTRK pin input during this time period. Hence, capacitance values less than approximately 2200pF will not significantly affect soft-start behavior.

When driving the SSTRK pin from another source, each channel's output can be set up to either coincidentally or ratiometrically track another supply's output, as shown in Figure 16. In the following discussions, V_{OUT1} refers to the VE2266/VE2266A output 1 as a master channel and V_{OUT2} refers to output 2 as a slave channel. In practice, either channel can be used as the master.

To implement the coincident tracking in Figure 16a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the SSTRK pin of the slave channel. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in a. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking, the feedback pin of the master channel should connect to the SSTRK pin of the slave channel (as in Figure 17b). By selecting different resistors, the VE2266/VE2266A can achieve different modes of tracking including the two in Figure17.

Upon start-up, the regulator defaults to PFM Mode operation until the output exceed 80% of its final value (V_{FB} > 0.48V). Once the output reaches this voltage, the operating mode of the regulator switches to the mode selected by the MODE/SYNC pin as described above. During normal operation, if the output drops below 10% of its final value (as it may when tracking down, for instance), the regulator will automatically switch to PFM Mode

operation to prevent inductor saturation and improve SSTRK pin accuracy.

Output Power Good

The PG output of the VE2266/VE2266A is driven by a 50Ω (typical) open-drain pull-down device. This device will be turned off once the output voltage is within 5% (typical) of the target regulation point, allowing the voltage at PG to rise via an external pull-up resistor. If the output voltage exits an 8% (typical) regulation window around the target regulation point, the open-drain out- put will pull down with 50Ω output resistance to ground, thus dropping the PG pin voltage. This behavior is described in Figure 18.

A filter time of 40μs (typical) acts to prevent unwanted PG output changes during V_{OUT} transient events. As a result, the output voltage must be within the target regulation window of 5% for 40μs before the PG pin pulls high. Conversely, the output voltage must exit the 8% regulation window for 40μs before the PG pin pulls to ground.

Efficiency Considerations

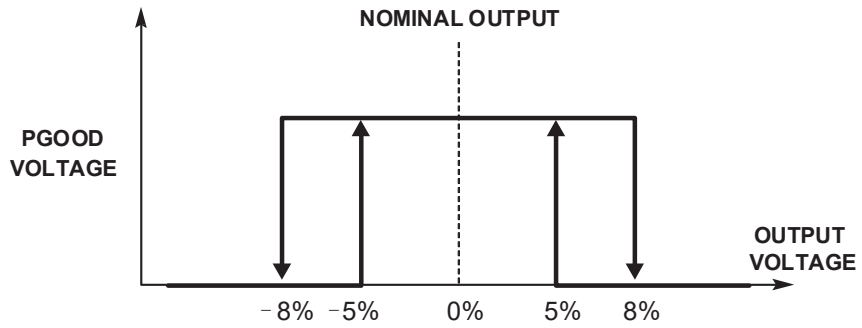


Figure 18. PGOOD Pin Behavior

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

% Efficiency = 100% – (L1 + L2 + L3 +…)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in VE2266/VE2266A circuits: 1) I^2R losses, 2) switching losses and quiescent power loss, 3) transition losses and other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is “chopped” between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = R_{DS(ON)TOP}DC + R_{DS(ON)BOTTOM}(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

$$I^2R\ losses = I_{OUT}^2(R_{SW} + R_L)$$

2. The internal LDO draws power from the V_{IN} input to regulate the V_{CC} rail. The total power loss here is the

sum of the switching losses and quiescent current losses from the control circuitry.

Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{CC} that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f (Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. For estimation purposes, the gate charges (QT + QB) on each VE2266 regulator channel are approximately 7.5nC.

To calculate the total power loss from the LDO load, simply add the gate charge current and quiescent cur- rent and multiply by the voltage applied to V_{IN}:

$$P_{LDO} = (I_{GATECHG} + I_Q) \cdot V_{IN}$$

3. Other “hidden” losses such as transition loss, copper trace resistances, and internal load currents can account for additional efficiency degradations in the overall power system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The VE2266/VE2266A internal power devices switch quickly enough that these losses are not significant compared to other sources.

Other losses, including diode conduction losses during dead-time and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

The VE2266/VE2266A requires the ground pins to be well soldered to the PC board to provide good thermal contact. This gives the QFN package exceptional thermal properties, which is necessary to prevent excessive self- heating of the part in normal operation.

In a majority of applications, the VE2266/VE2266A does not dissipate much heat due to its high efficiency and low thermal resistance of its QFN package. However, in applications where the VE2266/VE2266A is running at high ambient temperature, high input supply voltage, high switching frequency, and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off until temperature returns to 150°C.

To prevent the VE2266/VE2266A from exceeding the maximum junction temperature of 125°C, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \cdot \theta_{JA}$$

As an example, consider the case when one of the regulators is used in an application where V_{IN} = 12V, I_{OUT} = 6A, frequency = 1MHz, V_{OUT} = 1.8V. From the $R_{DS(ON)}$ graphs in the Typical Performance Characteristics section, the top switch on-resistance is nominally 36mΩ and the bottom switch on-resistance is nominally 19mΩ at 50°C ambient. The equivalent power MOSFET resistance R_{SW} is:

$$R_{DS(ON)TOP} \cdot \frac{1.8V}{12V} + R_{DS(ON)BOTTOM} \cdot \frac{10.2V}{12V} = 21.6m\Omega$$

From the previous section’s discussion on gate drive, we estimate the total gate drive current through the LDO to be 1MHz • 7.5nC = 7.5mA, and IQ of one channel is 0.65mA (see Electrical Characteristics). Therefore, the total power dissipated by a single regulator is:

$$P_D = {I_{OUT}}^2 \cdot R_{SW} + (I_{GATECHG} + I_Q) \cdot V_{IN}$$
$$P_D = (6A)^2 \cdot (0.0216\Omega) + (7.5mA + 0.65mA) \cdot (12V)$$
$$= 0.874W$$

Running two regulators under the same conditions would result in a power dissipation of 1.748W. The QFN

5mm× 4mm package junction-to-ambient thermal resistance, θ_{JA}, is around 21°C/W. Therefore, the junction temperature of the regulator operating in a 50°C ambient temperature is approximately:

$$T_J = 1.748W \cdot 21\,℃/W + 50℃ = 87℃$$

which is below the maximum junction temperature of 125°C. With higher ambient temperatures, a heat sink or cooling fan should be considered to drop the junction-to- ambient thermal resistance.

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 50°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 15% at 87°C yields a new junction temperature of 92°C. If the application calls for a higher ambient temperature and/or higher load currents, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow. Figure 19. is a temperature derating curve based on the demo board. It can be used to estimate the maximum allowable ambient temperature for given DC load currents in order to avoid exceeding the maximum operating junction temperature of 125°C.

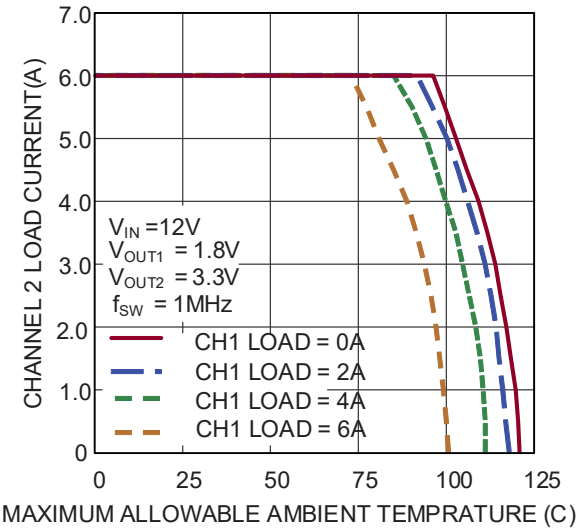


Figure 19. Temperature Derating Curve for Demo Circuit

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the VE2266/VE2266A. Check the following in your layout:

1) Do the input capacitors connect to the V_{IN} and GND pins as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.

2) The output capacitor, C_{OUT}, and inductor L should be closely connected to minimize loss. The (–) plate of C_{OUT} should be closely connected to both GND and the (–) plate of C_{IN}.

3) The resistive divider, (e.g. R1 to R4 in Figure 17.) must be connected between the (+) plate of C_{OUT} and a ground line terminated near GND. The feedback signal FB should be routed away from noisy components and traces, such as the SW line, and its trace length should be minimized. Keep R1 and R2 close to the IC.

4) Keep sensitive components away from the SW pin. The RT resistor, the compensation components, the feedback resistors, and the V_{CC} bypass capacitor should all be routed away from the SW trace and the inductor L.

5) A ground plane is preferred.

6) Flood all unused areas on all layers with copper in order to reduce the temperature rise of power components. These copper areas should be connected to the exposed backside of the package (GND).

Refer to Figure 21. for board layout examples.

Design Example

As a design example, consider using the VE2266 in an application with the following specifications: $V_{IN(MAX)}$ = 13.2V, V_{OUT1} = 1.8V, V_{OUT2} = 3.3V, $I_{OUT(MAX)}$ = 6A, $I_{OUT(MIN)}$ = 10mA, f = 2MHz, V_{DROOP}~(5% • V_{OUT}). The following discussion will use equations from the previous sections.

Because efficiency is important at both high and low load current, PFM Mode operation will be utilized.

First, the correct RT resistor value for 2MHz switching frequency must be chosen. Based on the equation discussed earlier, RT should be 160k; the closest standard value is 162k. RT can be tied to V_{CC} if switching frequency accuracy is not critical.

Next, determine the channel 1 inductor value for about 40% ripple current at maximum V_{IN}:

$$L1 = \left(\frac{1.8V}{2MHz \cdot 2.4A}\right)\left(1 - \frac{1.8V}{13.2V}\right) = 0.32\mu H$$

A standard value of 0.33μH should work well here. Solving the same equation for channel 2 results in a 0.47μH inductor.

C_{OUT} will be selected based on the charge storage requirement. For a V_{DROOP} of 90mV for a 6A load step:

$$C_{OUT} \cong \frac{3 \cdot \Delta I_{OUT}}{f \cdot V_{DROOP}} = \frac{3 \cdot (6A)}{(2MHz) \cdot (90mV)} = 100\mu F$$

Two 47μF ceramic capacitor should be used for channel 1. Solving the same equation for channel 2 (using 5% of V_{OUT} for V_{DROOP}) results in 55μF of capacitance (47μF is the closest standard value).

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 6A \cdot \frac{\sqrt{1.8V(13.2V - 1.8V)}}{13.2V} = 2.1A$$

Solving this equation for channel 2 results in an RMS input current of 2.8A. Decoupling each V_{IN} input with a 47μF ceramic capacitor should be adequate for most applications. Lastly, the feedback resistors must be chosen. Picking R1 and R3 to be 13.7k, R2 and R4 are calculated to be:

$$R2 = (13.7k) \cdot \left(\frac{1.8V}{0.6V} - 1\right) = 27.4k$$

$$R4 = (13.7k) \cdot \left(\frac{3.3V}{0.6V} - 1\right) = 61.9k$$

The final circuit is shown in Figure 20.

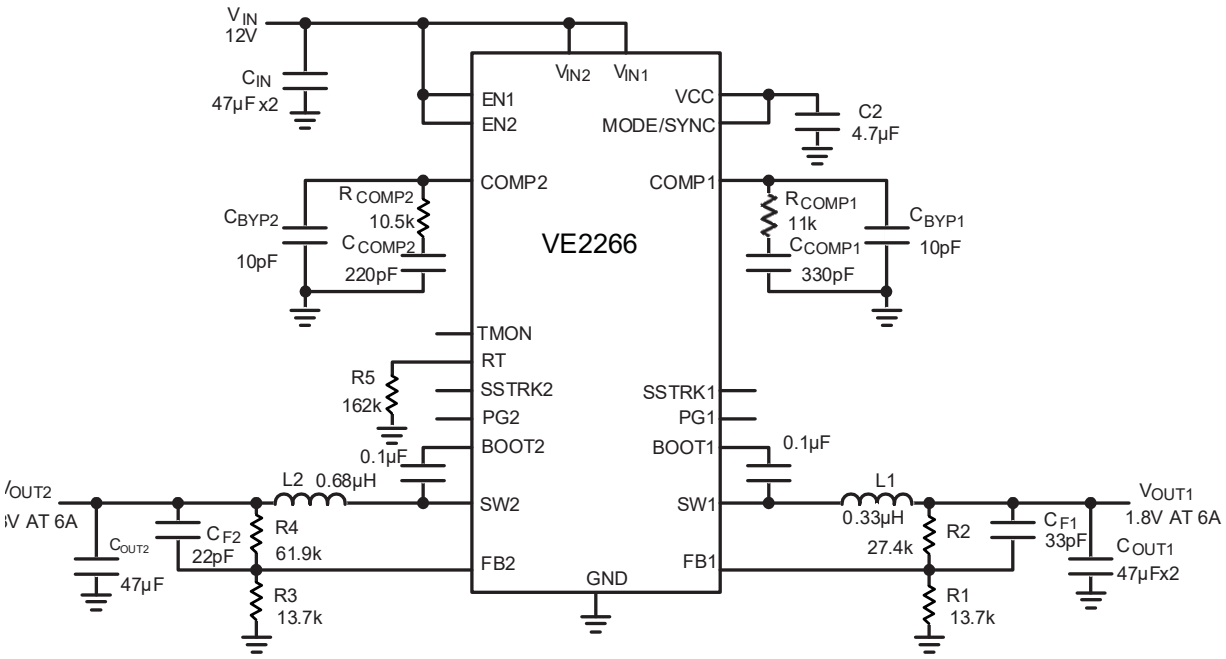


Figure 20. Design Example Circuit

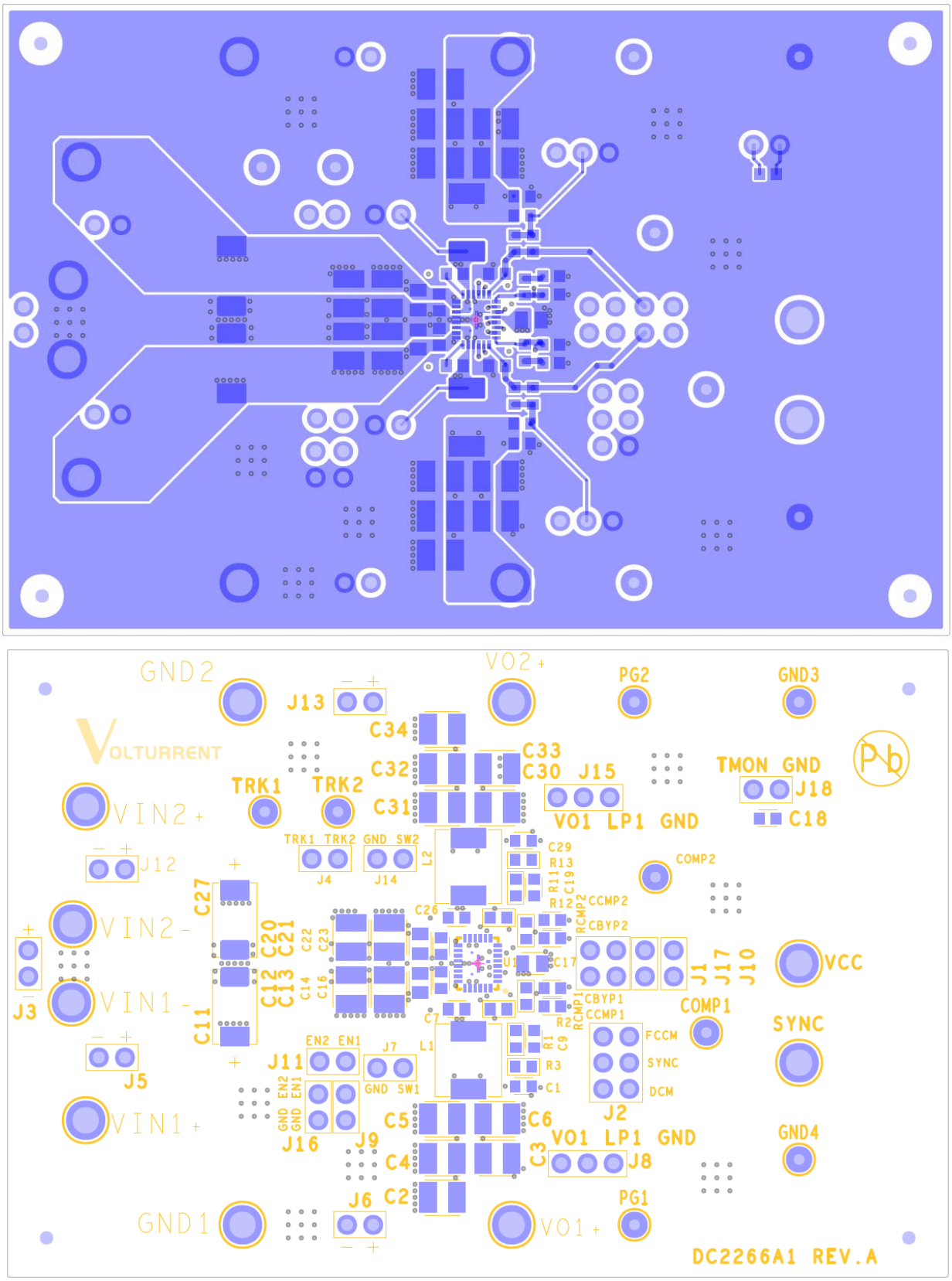
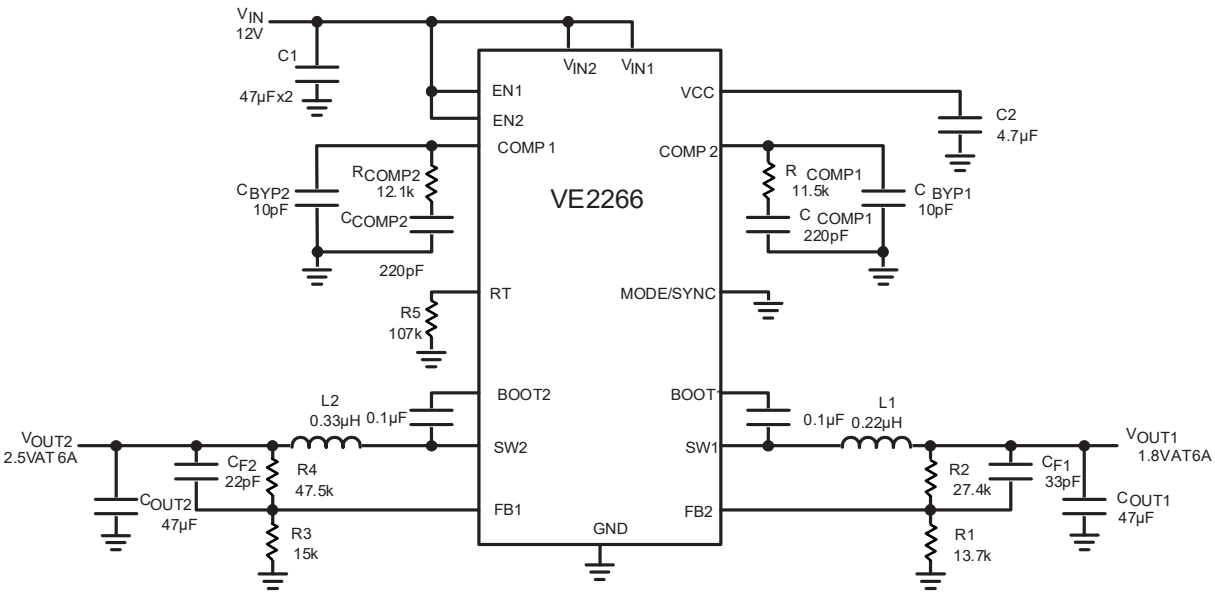
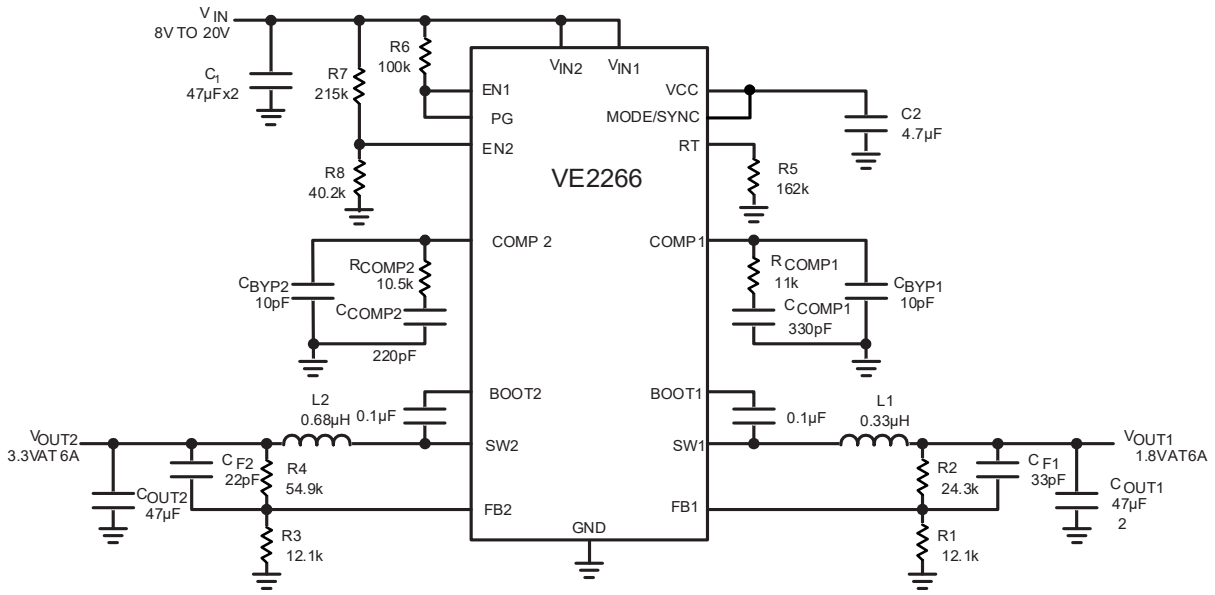


Figure 21. Recommended PCB Layouts

TYPICAL APPLICATION CIRCUITS

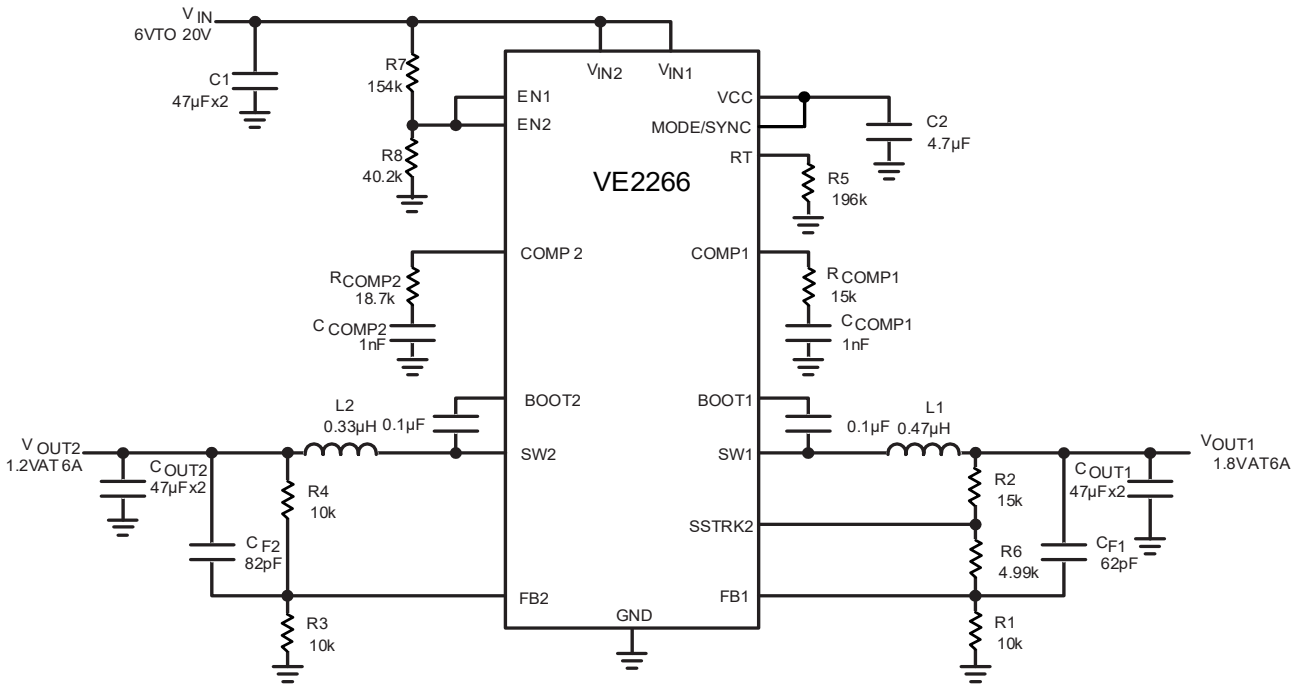


1.8V/2.5V 3MHz Buck Regulator

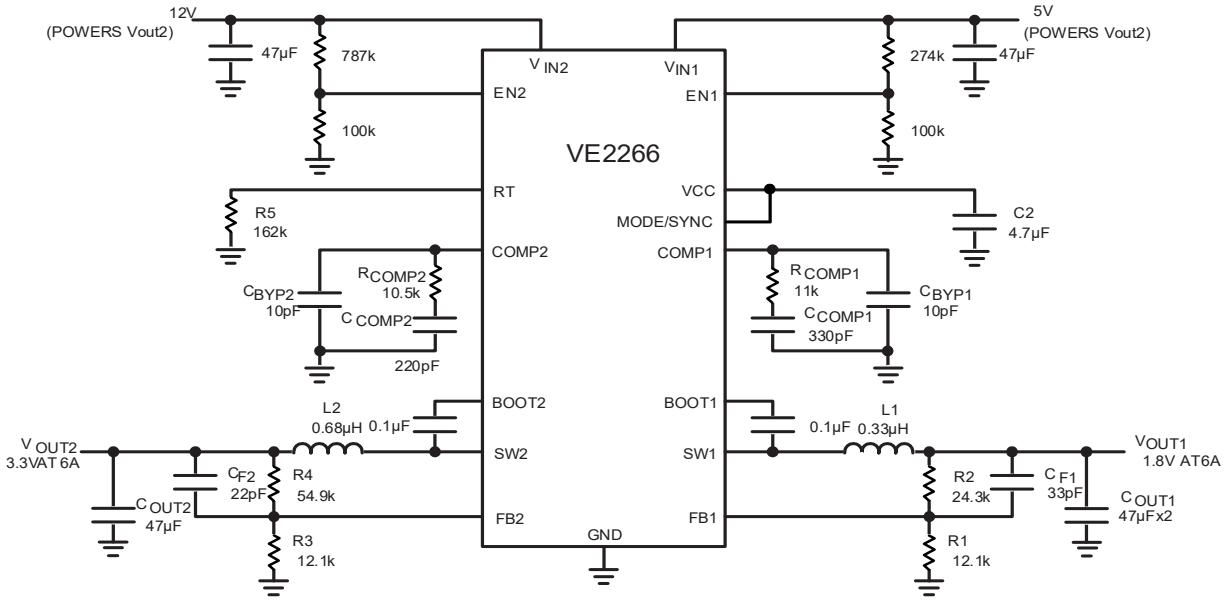


3.3V/1.8V Sequenced Regulator with 8V Input UVLO (V_{OUT1} Enabled After V_{OUT2})

TYPICAL APPLICATION CIRCUITS



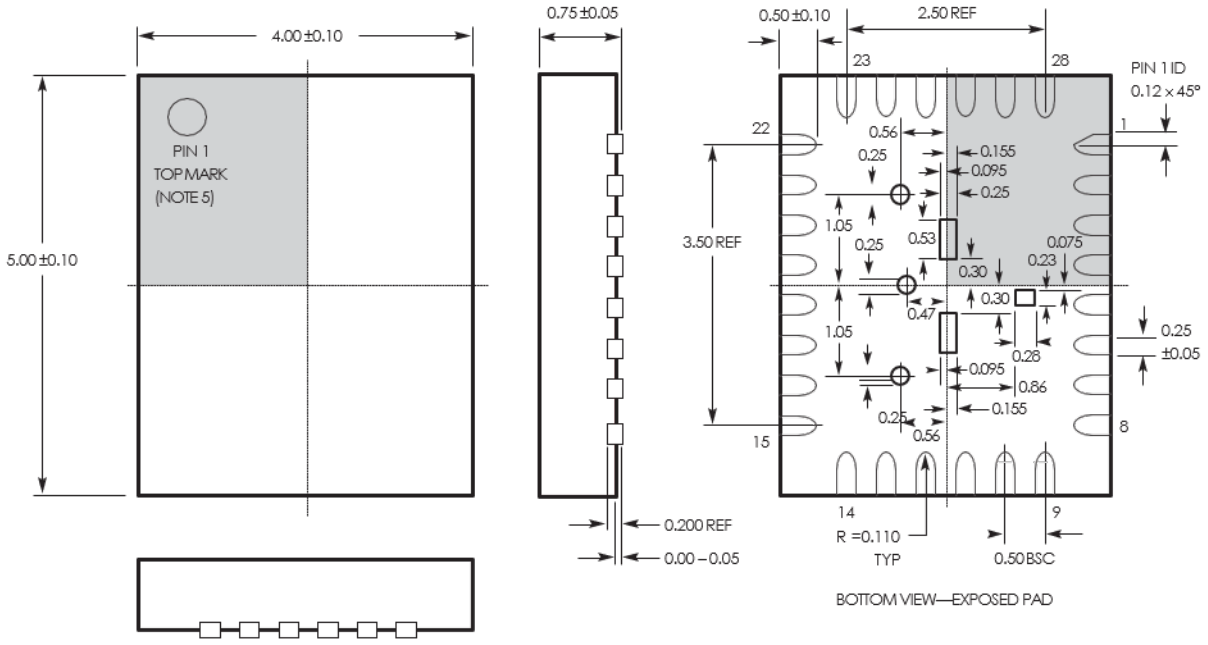
1.2V/1.8V Buck Regulator with Coincident Tracking and 6V Input UVLO



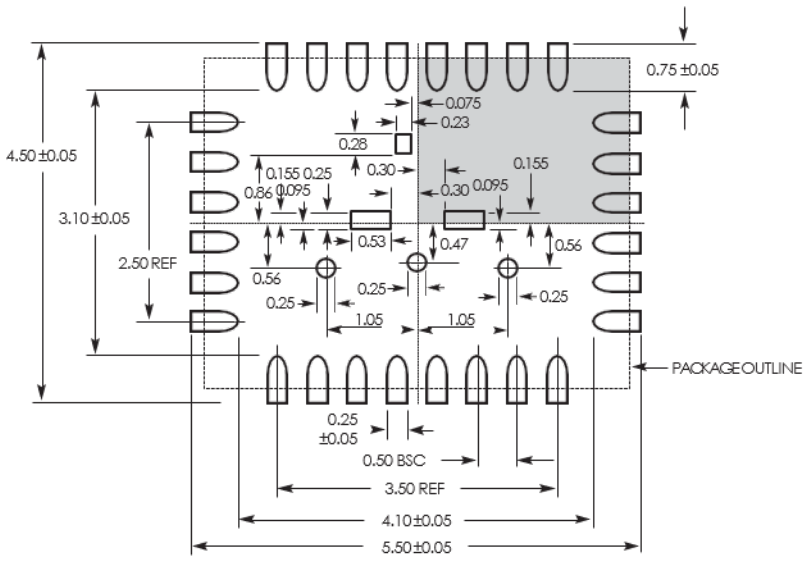
Dual Output Regulator from Multiple Input Supplies (Powers V_{IN1} Before V_{IN2})

PACKAGE INFORMATION

28-Lead Plastic QFN(4mmx5mm)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

REVISION HISTORY

Revision	Data	Description
1.0	2024-10-18	Initial Release