36V, 3.5A, Low IQ, Synchronous Step-Down Converter

DESCRIPTION

The VE2430Q is a high-frequency, synchronous, step-down converter. It offers a very compact solution that achieves 3.5A of continuous output current with excellent load and line regulation over a wide 3.3V to 36V input range. The switching frequency can be programmed or synchronized to an external clock. The synchronous operation and ultralow 21μA sleep mode quiescent current provide high efficiency over the output current load range, allowing the VE2430Q to be used in a variety of step-down applications in automotive and battery-powered applications.

Peak-current-mode operation provides fast transient response and eases loop stabilization. The excellent low dropout performance allows the VE2430Q to be used in high duty cycle applications.

Full protection features include over-current and short-circuit protection, and thermal shutdown. An open-drain power good (PG) signal indicates when the output is within 10% of its nominal voltage.

The VE2430Q is available in a space-saving FCQFN3X4-16 (3mm x 4mm Wettable Flank) package.

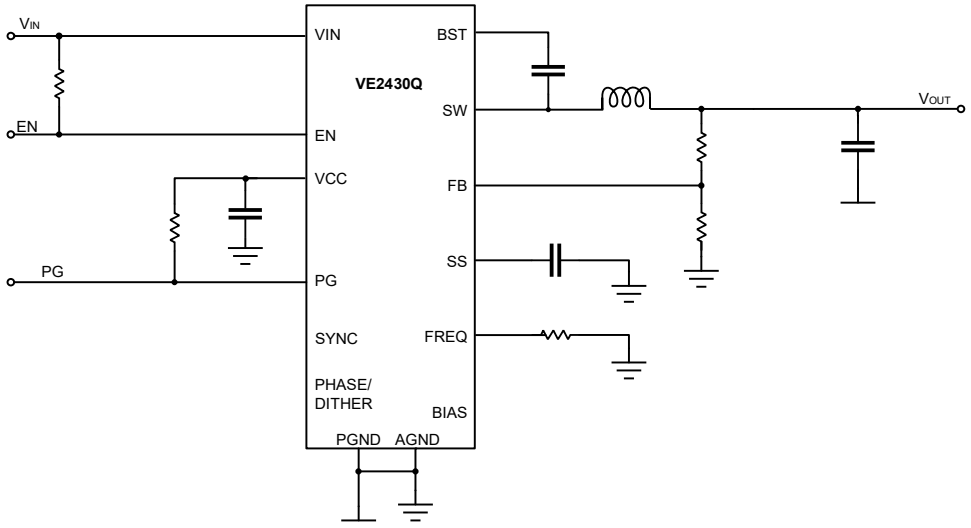
FEATURES

- 2μA Low Shutdown Supply Current
- 21μA No-Load Quiescent Current
- Internal 125mΩ High-Side and 55mΩ Low-Side MOSFET
- 350kHz to 2.5MHz Programmable Switching Frequency
- Power Good (PG) Output
- External Soft Start (SS)
- 80ns Minimum On Time
- 120ns Minimum Off Time
- Selectable Forced PWM and PFM Mode
- Selectable dither or non-dither mode for EMI
- Hiccup Over-Current Protection (OCP)
- AEC-Q100 Grade-1
- Available in a FCQFN3X4-16 (3mm x 4mm Wettable Flank) package

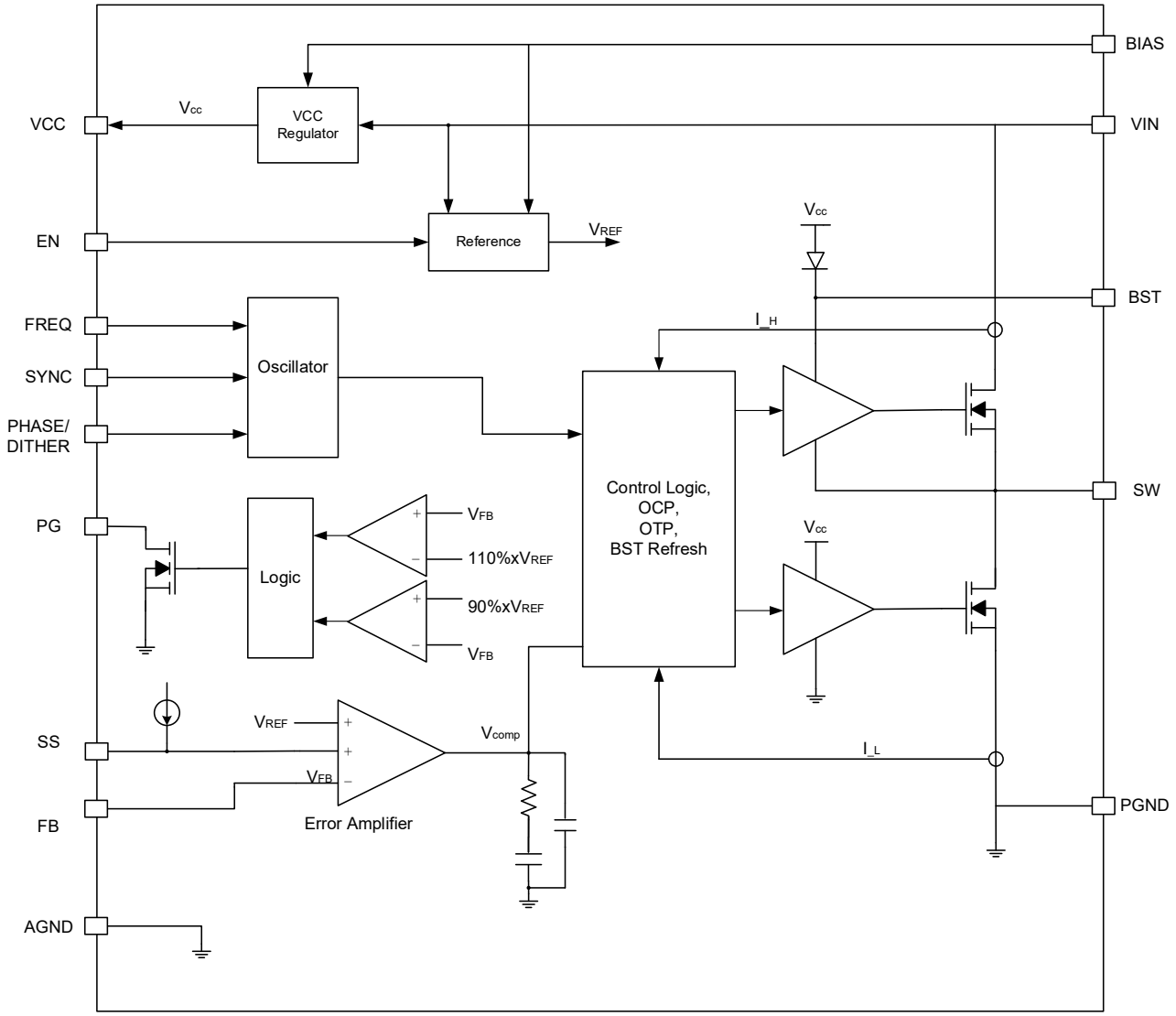
APPLICATIONS

- Automotive Systems
- Industrial Control Systems

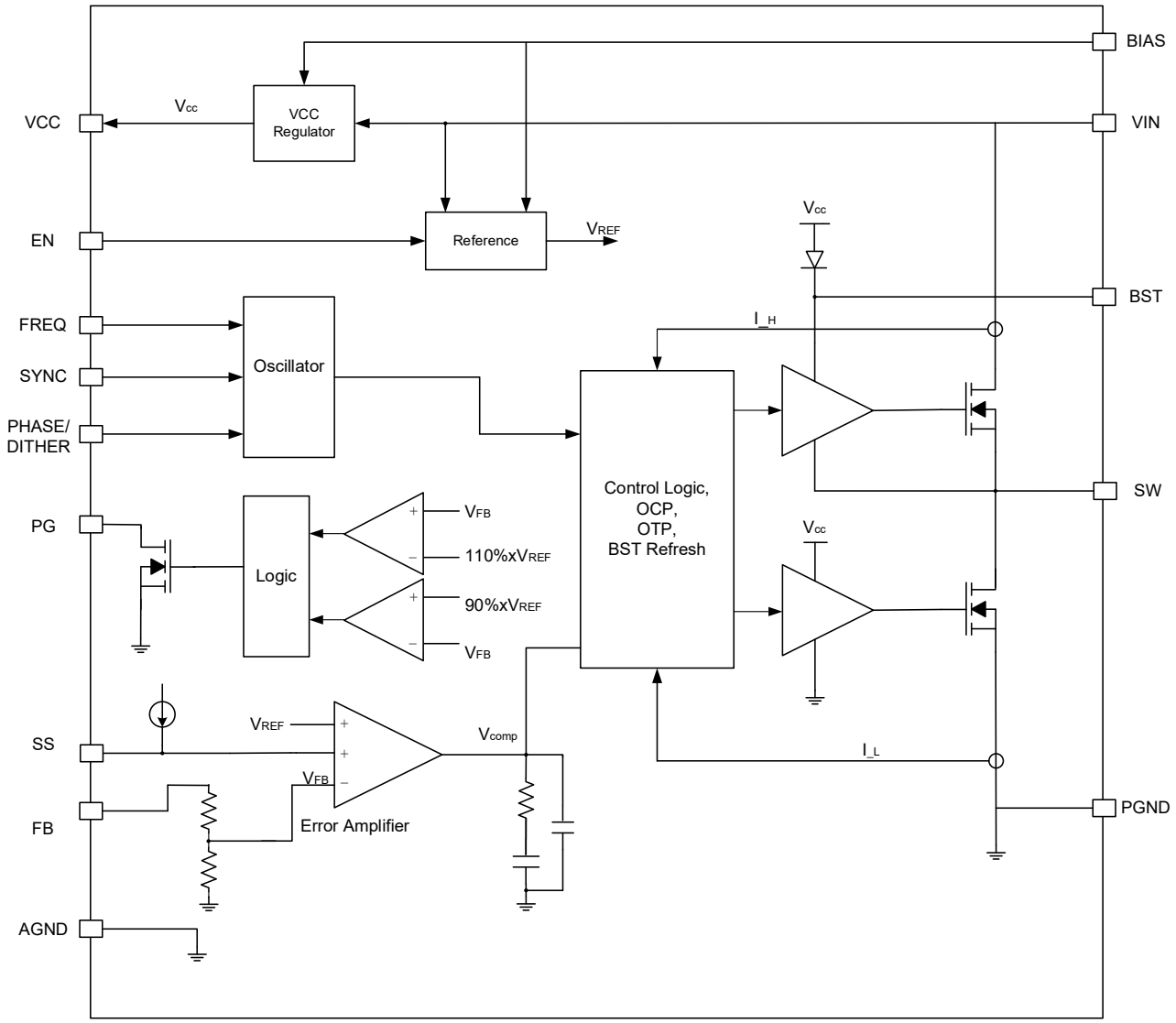
TYPICAL APPLICATION



BLOCK DIAGRAM



Block Diagram Fixed Output

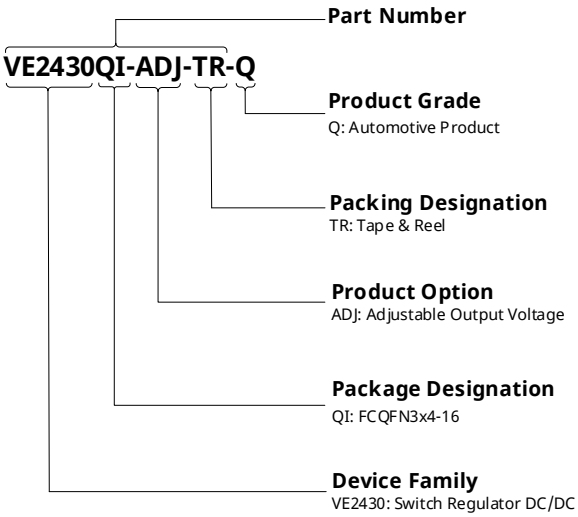


Block Diagram Adjustable Output

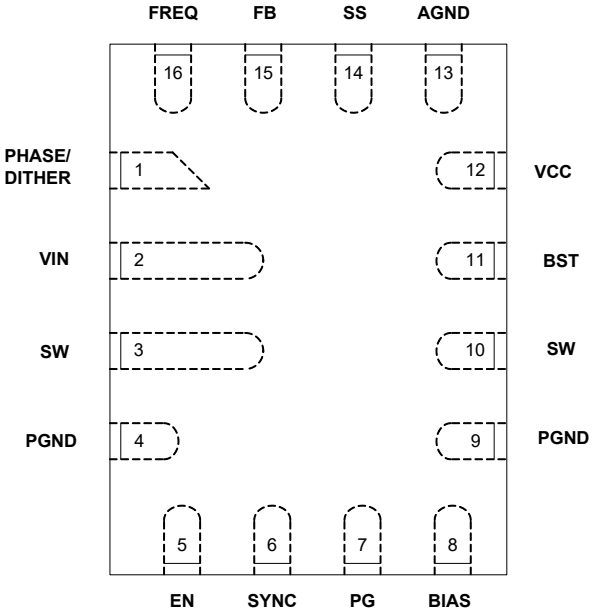
ORDERING INFORMATION

Ordering Information	Mark	Option	Class (1)	Temperature Range	Package	Pack	Quantity
VE2430QI-ADJ-TR-Q	2430Q	ADJ	Q	-40 to +125°C	FCQFN3x4-16	TR	5000

Note 1: The Class definition, Q=Automotive.



PIN CONFIGURATIONS



FCQFN3x4-16

PIN DESCRIPTION

Name	FCQFN3X4-16	Description
PHASE / DITHER	1	Selectable in-phase or 180° out-of-phase of SYNC input when pull PHASE/DITHER pin high or low. Pull high to be in-phase. Pull low to be 180° out-of-phase. When the voltage of this pin is between 0.7V and (V_{CC} - 0.3) V or floating this pin before soft start, the dither function will be enabled. Dither function is only valid under FPWM mode.
VIN	2	Input supply. VIN supplies power to all of the internal control circuitries and the power train. Place a decoupling capacitor to ground close to VIN to minimize switching spikes.
SW	3,10	Switch node. SW is the output of the internal power switches. Pin 3 and Pin 10 are internally connected.
PGND	4,9	Power ground. PGND is the reference ground of the power device and requires careful consideration during PCB layout. For best results, connect PGND with copper pours and vias.
EN	5	Enable. Pull EN below the specified threshold to shut the chip down. Pull EN above the specified threshold to enable the chip.
SYNC	6	Synchronize. Apply a 350kHz to 2.5MHz clock signal to SYNC to synchronize the internal oscillator frequency to the external clock. The external clock should be at least 250kHz larger than the R_{FREQ} set frequency. SYNC can also be used to select forced PWM mode (FPWM) or PFM Mode. Before the chip starts up, drive SYNC low or leave SYNC floating to choose PFM mode, and drive SYNC high to external power source or pull up SYNC to VCC directly to set the part in forced PWM mode.
PG	7	Power good output. The output of PG is an open drain. Float PG if not used.
BIAS	8	Bias input. Connect BIAS to an external power supply (5V ≤ VBIAS ≤ 18V) to reduce power dissipation and increase efficiency. If not in use, float BIAS or connect BIAS to ground.
BST	11	Bootstrap. BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BST and SW.
VCC	12	Bias supply. VCC supplies power to the internal control circuit and gate drivers. A decoupling capacitor (≥1μF) to ground is required close to VCC.
AGND	13	Analog ground. AGND is the reference ground of the logic circuit.
SS	14	Optional external soft-start time setting. Connect an external capacitor between this pin and GND to set soft-start time externally. The VE2430Q sources 10μA from SS to the soft-start capacitor during start-up. As the SS voltage rises, the feedback threshold voltage increases to limit inrush

Name	FCQFN3X4-16	Description
		current during start-up. Floating the pin will activate the internal 0.7ms soft-start setting.
FB	15	Feedback input. For adjustable output version, connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces. For fixed output version, connect FB pin to the output directly.
FREQ	16	Switching frequency program. Connect a resistor from FREQ to ground to set the switching frequency.

ABSOLUTE MAXIMUM RATINGS

Parameter	Minimum	Maximum	Unit
VIN	-0.3	+40	V
BST	-0.3	VIN+6.5	V
SW	-0.3	+40	V
SW (transient < 10 ns)	-2	+45	V
EN	-0.3	+40	V
PG	-0.3	+40	V
BIAS	-0.3	+20	V
All Other Pins	-0.3	+6	V
Junction Temperature		150	°C
Lead Temperature		260	°C
Storage Temperature	-65	150	°C

ESD RATINGS

Parameter	Value	Unit
Human Body Model (HBM), per AEC-Q100-002	2	kV
Charged Device Model (CDM), per AEC-Q100-011	1	kV
Latch-Up, per AEC-Q100-004	100	mA

THERMAL INFORMATION

Thermal Resistance	θ_{JA}(°C/W)	θ_{JC}(°C/W)
FCQFN3X4-16 (3mm x 4mm)	48	11

RECOMMENDED OPERATINIG CONDITIONS

Parameter	Minimum	Maximum	Unit
Temperature	-40	+125	°C
VIN to GND	3.3	36	V

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_A = -40°C to +125°C, $T_A \le T_J \le$ +150°C, unless otherwise noted. Typical values are at T_A = +25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VIN quiescent current	I_Q	V_{FB} = 0.85V, no load, no switching, T_J = +25°C		21		μA
		V_{FB} = 0.85V, no load, no switching			50	μA
VIN shutdown Current	I_S	V_{EN} =0V		2	6	μA
VIN under-voltage lockout threshold rising	UVLO		2.4	2.8	3.2	V
VIN under-voltage lockout threshold hysteresis	$UVLO_{HYS}$			150		mV
EN rising threshold	V_{EN_RISING}		0.9	1.05	1.2	V
EN threshold hysteresis	V_{EN_HYS}			0.12		V
FB Voltage	V_{FB}	T_J = +25°C	0.792	0.8	0.808	V
			0.784	0.8	0.816	V
HS switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		125	165	mΩ
LS switch on resistance	R_{ON_LS}	V_{CC} = 5V		55	85	mΩ
Switching Frequency	F_{SW}	RT = 238kΩ or from syn clock	400	475	550	kHz
		RT = 96kΩ or from syn clock	850	1000	1150	kHz
		RT =30kΩ or from syn clock	2250	2500	2750	kHz
Minimum on time	T_{ON_MIN}			80		ns
SYNC input low voltage	V_{SYNC_LOW}				0.4	V
SYNC input high voltage	V_{SYNC_HIGH}		1.8			V
Peak Current limit	I_{LIMIT_HS}	Duty cycle = 40%	4.6	5.6	7.4	A
Valley Current limit	I_{LIMIT_LS}	V_{OUT} = 3.3V, L = 4.7μH	3.1	3.4	3.8	A
ZCD	I_{ZCD}			0.1		A
Reverse current limit	I_{LIMIT_R}			3		A
Switch leakage current	I_{SW_LKG}			0.01	1	μA
Soft-start current	I_{SS}	V_{SS} = 0.8V	5	10	15	μA
V_{CC} regulator	V_{CC}			4.8		V
V_{CC} load regulation		I_{VCC}			2	%
PG rising threshold	PG_{RISING}	V_{FB} rising	85	90	95	%
		V_{FB} falling	105	110	115	%
FB Voltage	$PG_{FALLING}$	V_{FB} rising	79	84	89	%
		V_{FB} falling	113.5	118.5	123.5	%
PG deglitch timer	$T_{PG\_DEGLITCH}$	PG from low to high		30		μs

Parameter	Symbol	Condition	Min	Typ	Max	Unit
		PG from high to low		50		μs
PG output voltage low	V_{PG_LOW}	I_{SINK} = 2mA		0.2	0.4	V
Thermal shutdown [1]	T_{SD}			150		°C
Thermal shutdown hysteresis	T_{SD_HYS}			20		°C

Notes:

[1] Not tested in production, guaranteed by design and characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, T_J = -40°C to +125°C, unless otherwise noted.

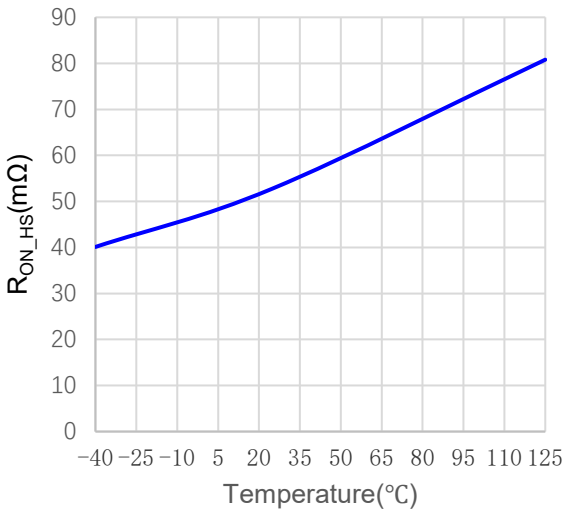


Figure 1. R_{ON-LS} vs Temp

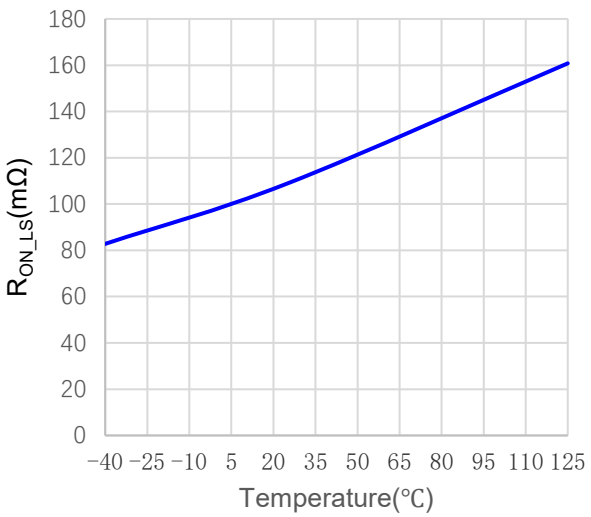


Figure 2. R_{ON-HS} vs Temp

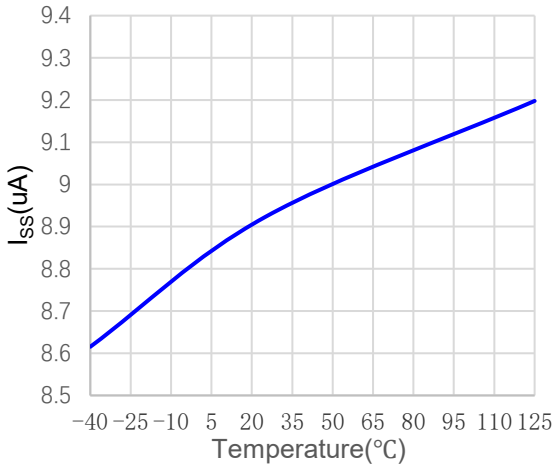


Figure 3. Soft-Start Current vs Temp

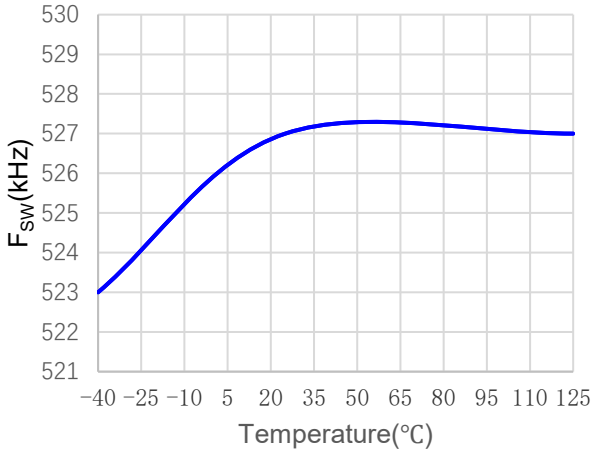


Figure 4. Fsw vs Temp

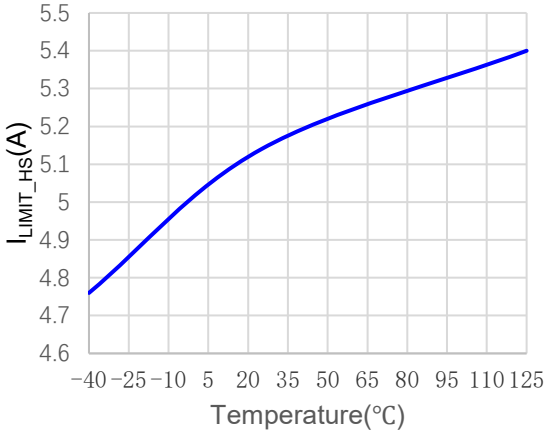


Figure 5. Peak Current vs Temp

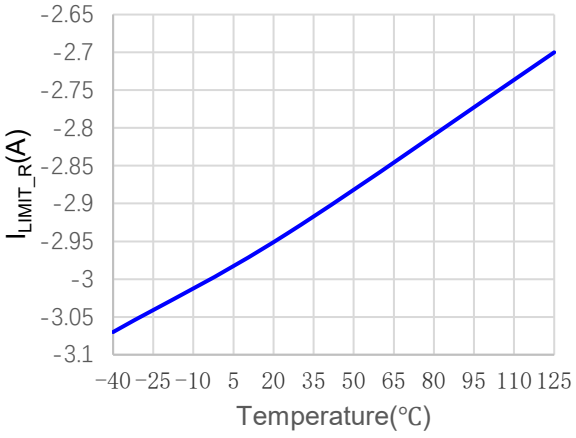


Figure 6. Reverse Current vs Temp

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, T_J = -40°C to +125°C, unless otherwise noted.

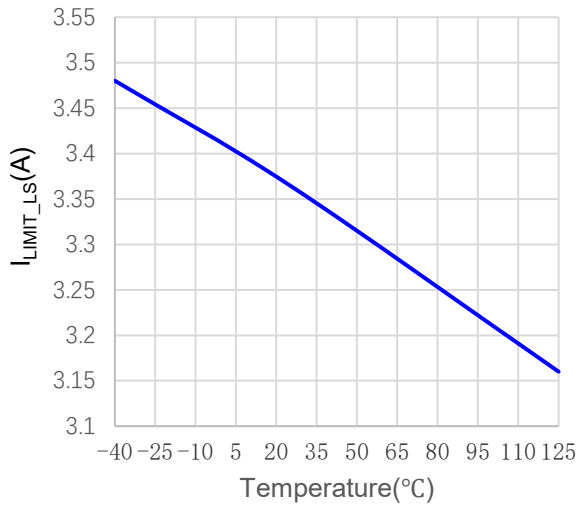


Figure 7. Valley Current vs Temp

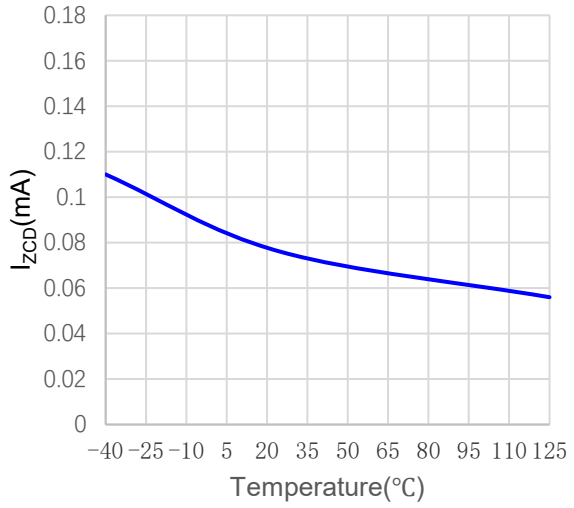


Figure 8. ZCD Current vs Temp

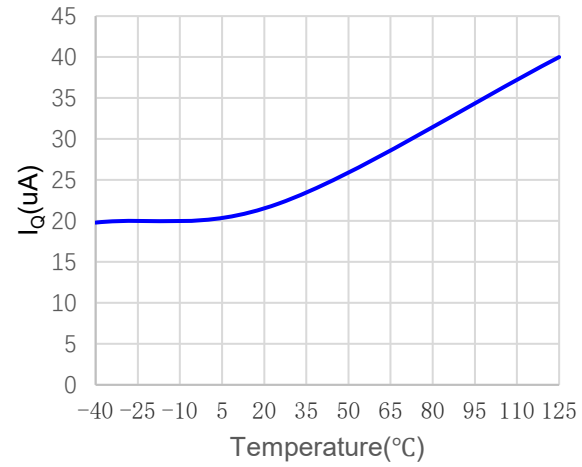


Figure 9. VIN quiescent current vs Temp

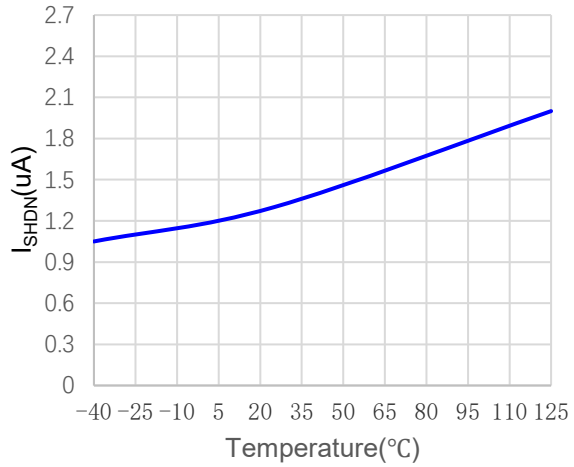


Figure 10. VIN shutdown Current vs Temp

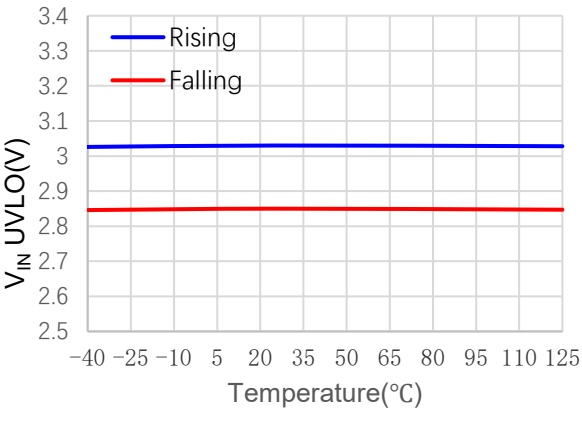


Figure 11. V_{IN} UVLO vs Temp

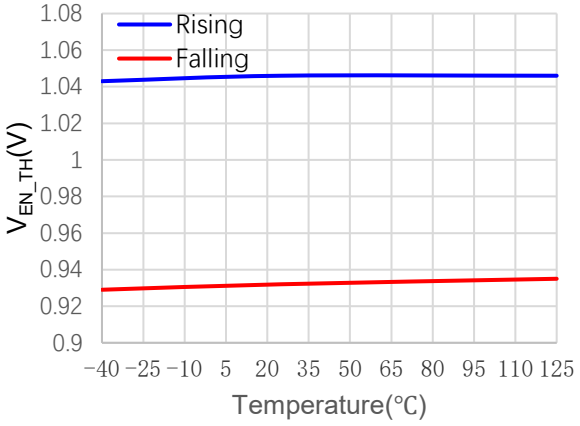


Figure 12. EN Threshold vs Temp

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, T_J = -40°C to +125°C, unless otherwise noted.

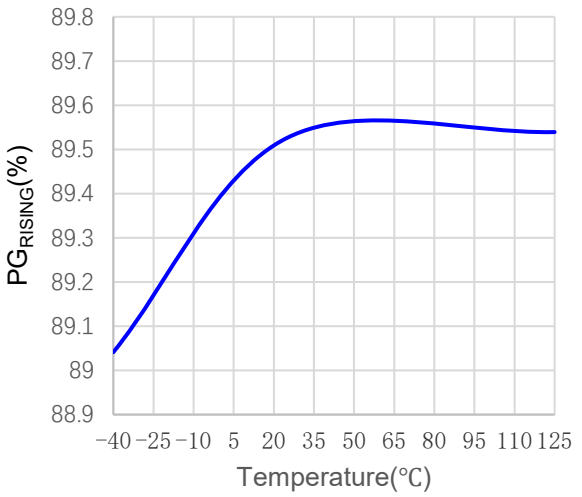


Figure 13. PG rising (FB rising) vs Temp

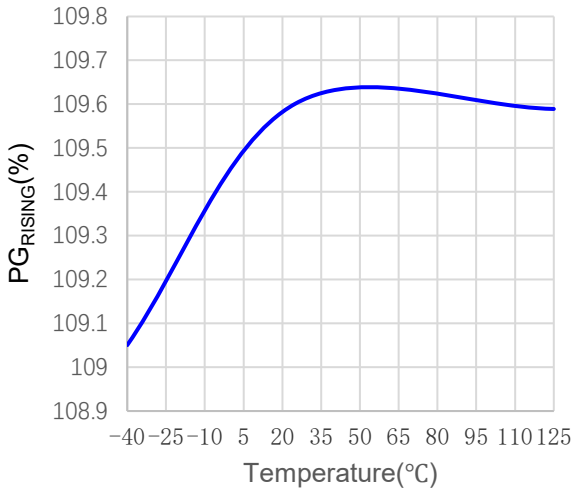


Figure 14. PG rising (FB falling) vs Temp

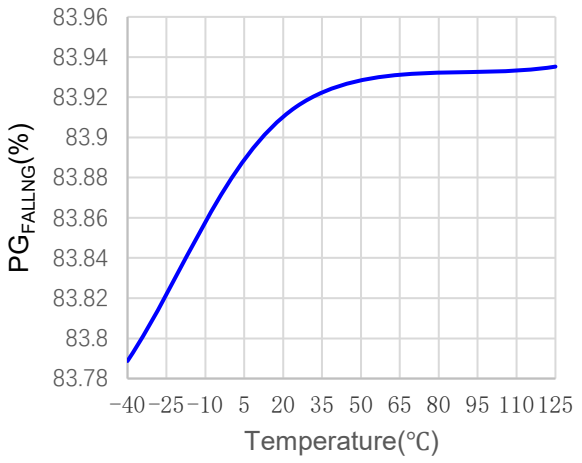


Figure 15. PG falling (FB falling) vs Temp

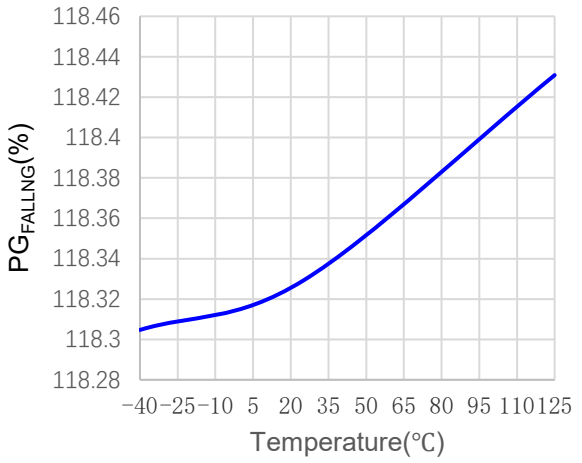


Figure 16. PG falling (FB rising) vs Temp

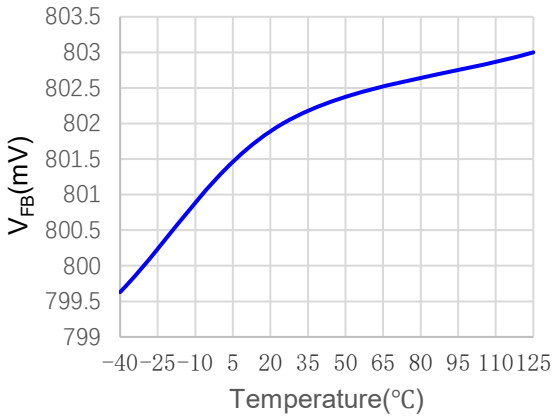


Figure 17. FB vs Temp

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=3.3V, L= 4.7uH,F_{SW}=500kHz, T_J = -40°C to +125°C, unless otherwise noted.

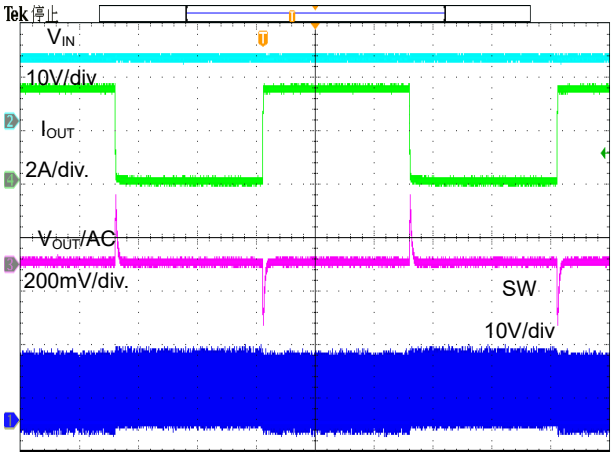


Figure 18. Load Transient 0-3.5A FPWM

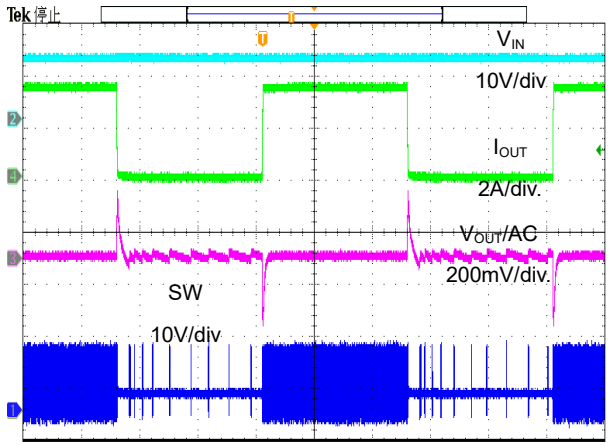


Figure 19. Load Transient 0-3.5A PFM

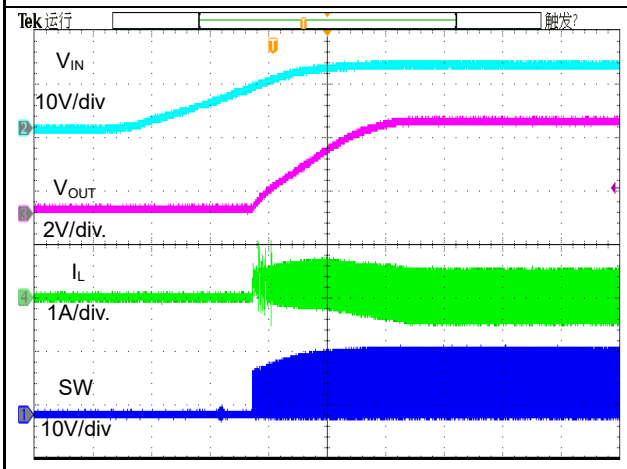


Figure 20. Soft Start 0A FPWM

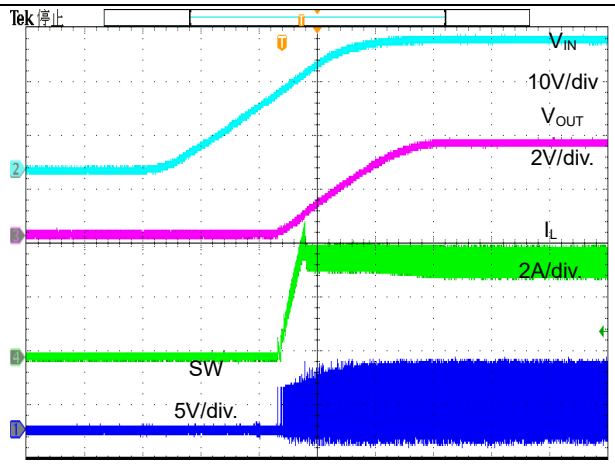


Figure 21. Soft Start 3.5A FPWM

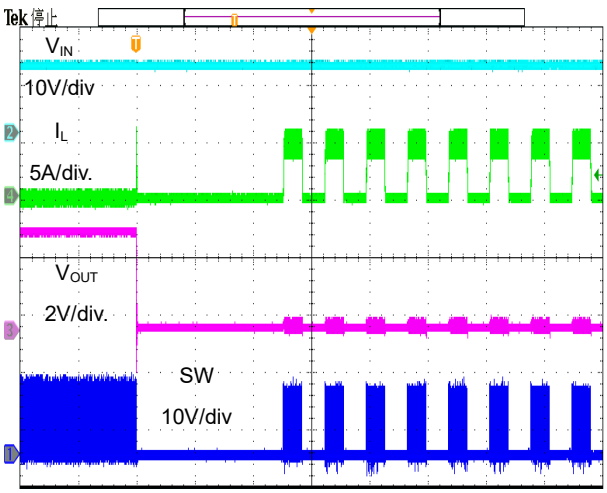


Figure 22. Hiccup OCP

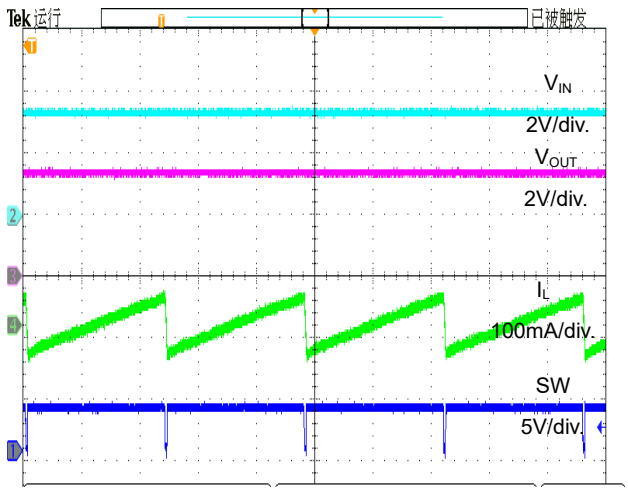


Figure 23. Low Drop Operation V_{IN}=3.2V

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=3.3V, L= 4.7uH,F_{SW}=500kHz,T_J = -40°C to +125°C, unless otherwise noted.

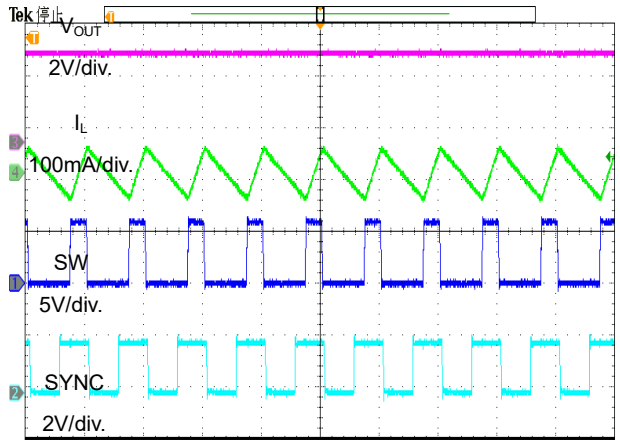


Figure 24. SYNC In-Phase

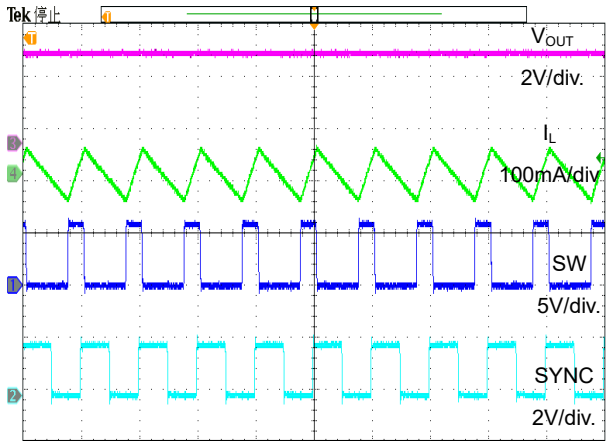


Figure 25. SYNC 180°

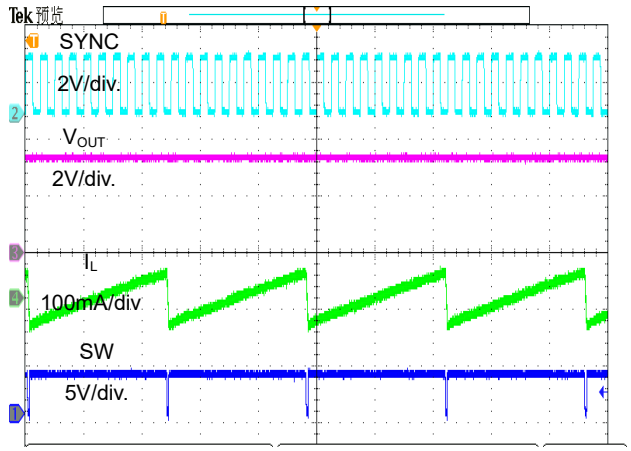


Figure 26. SYNC In Low Dropout

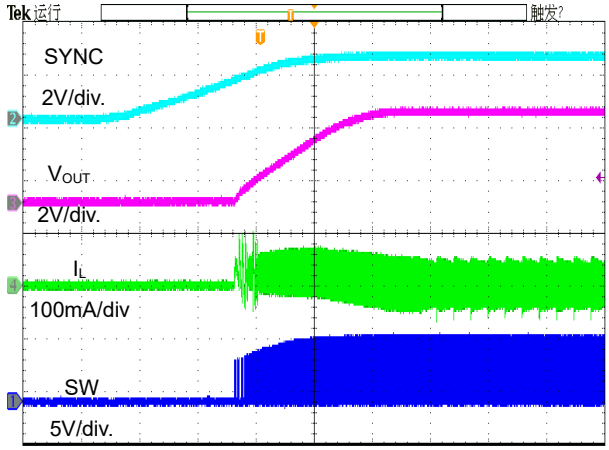


Figure 27. Start Up With Dither

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, F_{SW}=500kHz, FPWM,T_J = 25°C, unless otherwise noted.

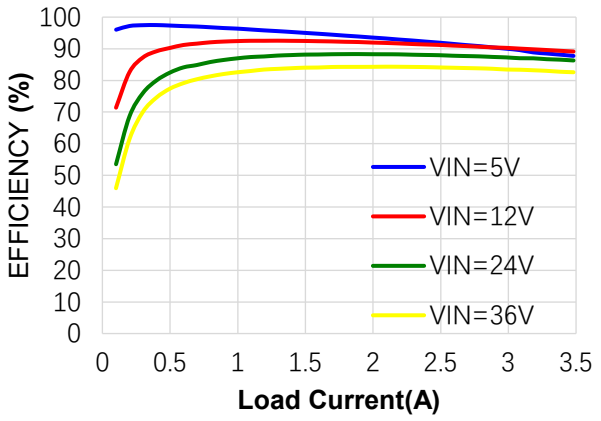


Figure 28. $5V_{OUT}$ Efficiency vs Load Current

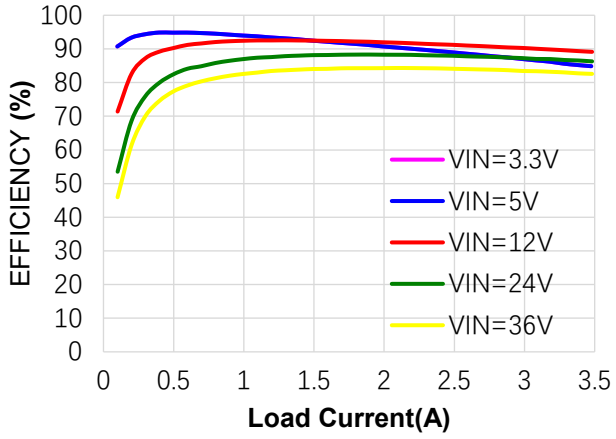


Figure 29. $3.3V_{OUT}$ Efficiency vs Load Current

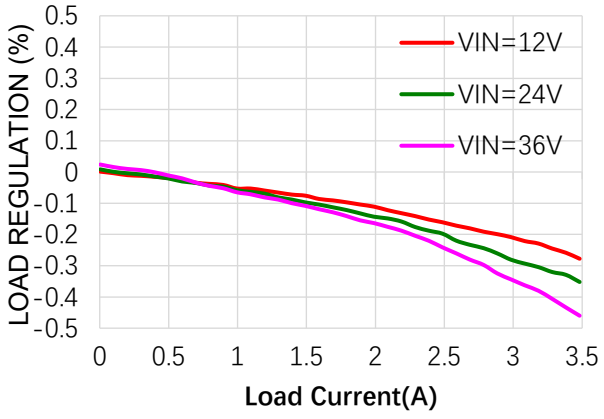


Figure 30. $5V_{OUT}$ Load Regulation

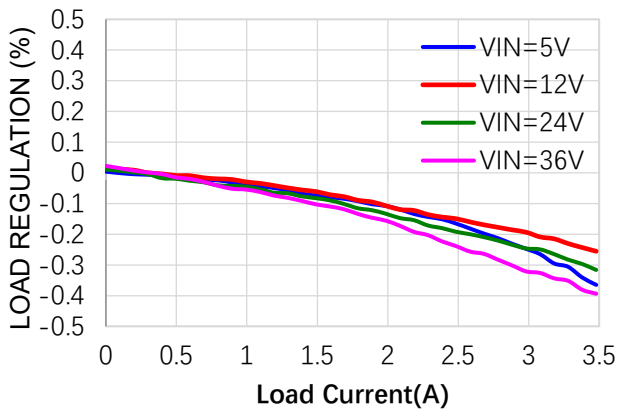


Figure 31. $3.3V_{OUT}$ Load Regulation

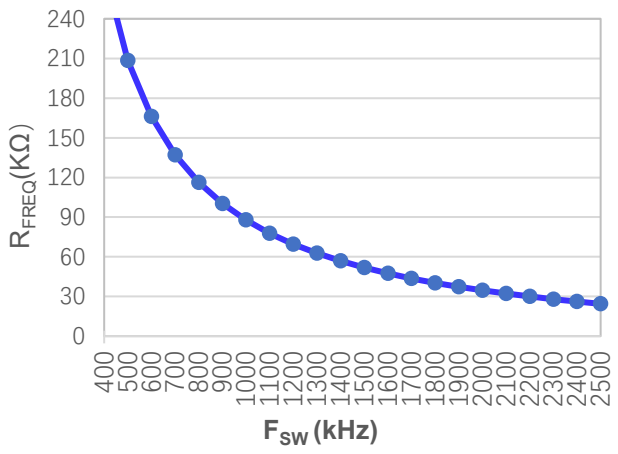


Figure 32. F_{SW} vs R_{FREQ}

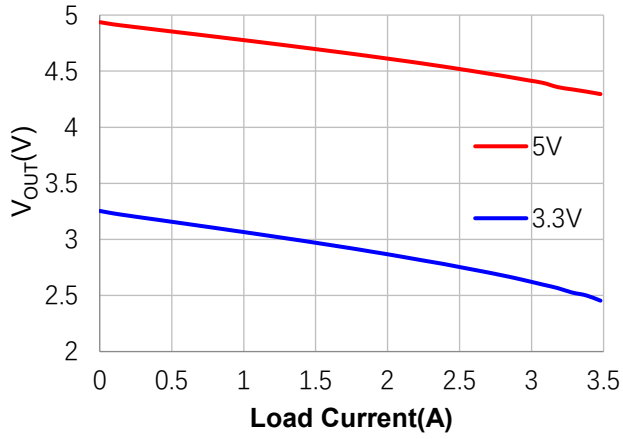


Figure 33. Output Voltage vs Load Current (Dropout Performance, V_{IN}=V_{OUT})

FUNCTION DESCRIPTION

General Description

The VE2430Q is a synchronous, step-down, switching regulator with integrated, internal, high-side and low-side power MOSFETs. The VE2430Q provides 3.5A of highly efficient output current with peak current mode control. The VE2430Q features a wide input voltage range, switching frequency is programmable from 350kHz to 2.5MHz, external soft start, and precision current limit. It's very low operational quiescent current makes it suitable for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate-to-high output currents, the VE2430Q operates in a fixed-frequency, peak current-control mode to regulate the output voltage. A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) is turned on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). If the current in the HSFET does not reach V_{COMP} in one PWM period, the HS-FET remains on, saving a turn-off operation. When the high-side power switch is off, the low side MOSFET (LS-FET) is turned on immediately and remains on until the next cycle begins. For each turn-on and -off in a switching cycle, the HS-FET turns on and off with a minimum on and off time limit.

PFM & FPWM Mode

The VE2430Q employs PFM mode functionality to optimize efficiency during light-load or no-load conditions. PFM mode can be enabled by connecting SYNC to a low level (0.4V) before start-up. SYNC can be used to synchronize switching after startup.

If Force PWM mode (FPWM) is enabled, the device is forced to work with a fixed frequency regardless of the output load current. The advantage of FPWM is the controllable frequency and smaller output ripple, but it also has low efficiency at light load (see Figure 34.).

If PFM mode is enabled, the VE2430Q enters non-synchronous operation for as long as the inductor current is approaching zero at light load. V_{COMP} drops below the PFM voltage, making the VE2430Q enter PFM mode. If the load is further decreased or is at no load, this puts the chip into sleep mode, which consumes very low quiescent current to further improve light-load efficiency.

When the load increases, and the DC value of V_{COMP} is higher than PFM voltage, the operation mode is discontinuous conduction mode (DCM) or FCCM, which have a constant switching frequency.

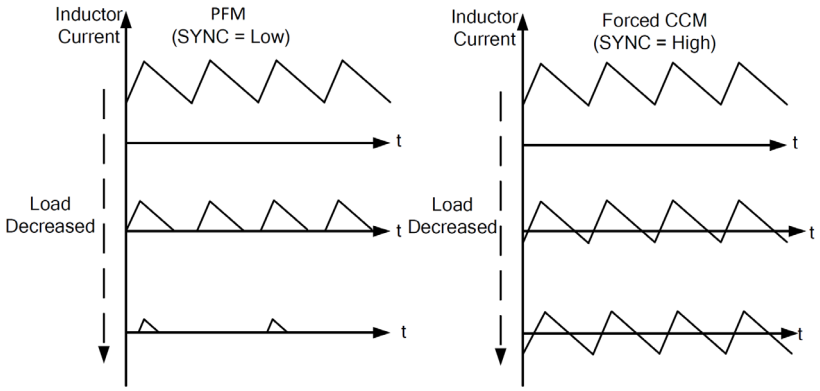


Figure 34. PFM Mode and Force PWM

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage with the internal reference (0.8V) and outputs a current proportional to the difference. This output current is used to charge or discharge the internal compensation network to form V_{COMP}, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Low Dropout Operation (BST Refresh)

In low dropout mode, the VE2430Q is designed to operate in low frequency mode as long as the off time is min-off time, improving dropout, increasing the effective duty cycle of the switching regulator. Low dropout operation makes the VE2430Q suitable for automotive cold-crank applications.

Internal Regulator

Most of the internal circuitry is powered on by the 4.8V internal regulator. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 4.8V, the output of the regulator is in full regulation. When V_{IN} is lower than 4.8V, the output degrades. For better thermal performance, connect BIAS to an external 5V source. V_{CC} and the internal circuit are powered by BIAS. Since there is an internal diode between BIAS and the internal circuit, float BIAS or connect BIAS to GND if it is not being used.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. When EN is pulled below its threshold voltage, the chip is put into the lowest shutdown current mode. Pulling EN above its threshold voltage turns on the part. Do not float EN.

Programmable Frequency (FREQ)

The VE2430Q oscillating frequency is programmed either by an external resistor (R_{FREQ}) from FREQ to ground or by a logic level SYNC signal. The value of R_{FREQ} can be calculated with Equation (1):

$$R_T(k\Omega) = \frac{400}{(4/(1000/F_{sw}-0.11)-0.325)} \qquad (1)$$

SYNC and PHASE

The chip can be synchronized to an external clock ranging from 350 kHz up to 2.5MHz through FREQ/SYNC. The internal oscillator frequency can be synchronized to an external clock ranging from 350kHz up to 2.5MHz through SYNC. The external clock should be at least 250kHz larger than the RFREQ set frequency. Ensure that the high amplitude of the SYNC clock is higher than 1.8V and the low amplitude is lower than 0.4V. There is no pulse width requirement, but there is always parasitic capacitance of the pad, so if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application.

PHASE is used when two or more VE2430Q devices are in parallel with the same SYNC clock. Pulling PHASE high forces the VE2430Q to operate in-phase of the SYNC clock. Pulling PHASE low forces the device to be 180° out-of-phase of the SYNC clock. By setting different voltages for PHASE, two devices can operate 180° out-of-phase to reduce the total input current ripple, so a smaller input bypass capacitor can be used (see Figure 35.).

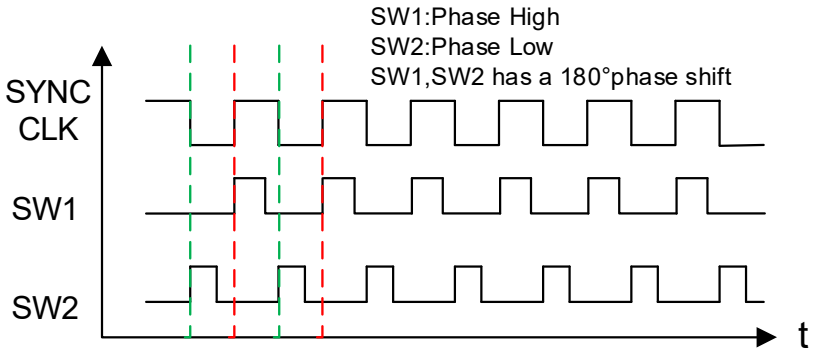


Figure 35. In-Phase and 180° Out-of-Phase

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, an internal current source begins charging the external soft-start capacitor. The internal V_{REF} voltage rises with the soft-start voltage (V_{SS}). V_{REF} rises from 0V to 0.8V, the output voltage ramps up from 0V to the regulated value following V_{REF} rising. When V_{SS} reaches 0.8V, and overrides the internal V_{REF}, so the error amplifier uses the internal V_{REF} as the reference. The soft-start time (T_{SS}) set by the external SS capacitor can be calculated with Equation (2):

$$T_{SS}(ms) = \frac{C_{SS}(nF)\times 1.1V}{I_{ss}(\mu A)} \qquad (2)$$

Where C_{SS} is the external SS capacitor, and ISS is the internal 10μA SS charge current.

There is also an internal fixed 700us soft start. The final SS time is determined by the longer time between 700us and the external SS setting time. SS can be used for tracking and sequencing.

Pre-Bias Start-Up

During start-up, if $V_{FB} > V_{REF}$ -150mV, then the output has a pre-bias voltage, and neither the HS-FET or LS-FET turn on until V_{REF} -150mV is higher than FB.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from running away thermally. When the silicon die temperature is higher than its upper threshold, the power MOSFETs are shut down. When the temperature is lower than its lower threshold, thermal shutdown is removed and the chip is enabled again.

Dither

When the voltage of PHASE/DITHER pin is between 0.3V and (Vcc – 0.7) V or floating before start up, the dither function is enabled, and dither function is only available in FCCM.

Hiccup Protection

When the output is shorted to ground, causing the output voltage to drop below 55% of its nominal output, the IC is shut down momentarily and begins discharging the soft start capacitor. The IC restarts with a full soft start when the soft-start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

Peak Current Protection

VE2430Q detects both high-side and low-side overcurrent using a cycle-by-cycle sensing method. Overcurrent in the high-side FET is detected by sensing the voltage across the FET while it is on. After the high-side FET is on, there is a noise blanking interval before the inductor current is compared to a fixed peak current threshold value of 5.6A. The high-side FET on-time is terminated immediately when the inductor current reaches 5.6A. The low-side FET is switched on to draw down the inductor current. The low-side FET remains on until the inductor current falls below a fixed threshold value of 3.4A. Overcurrent in the low-side FET is detected by sensing the voltage across the FET while it is on. After the low-side FET is on, there is a noise blanking time before the OC comparator is enabled. When the valley inductor current is below 3.4A, the high-side FET is allowed to turn on. Because of this, the cycle switching frequency is lower than the programmed switching frequency. The output voltage is reduced during OCP events. When the FB voltage falls to 55% of V_{REF}, VE2430Q enters into hiccup mode until the excessive load is removed.

For an application that operates near minimum on-time or if there is a hard short on the output, the COMP voltage moves higher to extend the on-time to respond to the lower output voltage. In this case, the high-side OCP dominates. When the output current ramps up gradually and the peak inductor current does not reach 5A, the low-side OCP dominates.

Negative Over Current Protection (NOC)

In FCCM, the PWM will controlled by the loop until the valley current reached negative current limitation. Once the valley current reached negative current limitation, LS FET will turning off immediately and HS FET will keep on until the current of HS FET reached 0A. And then start next cycle. It works in peak (0A) and valley (NOC) current mode.

Start-Up and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the rest of the circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for some to initialize the internal logic. During the initialization, the SS output is held low to ensure that the rest of the circuitries are ready before slowly ramping up.

Three events can shut down the chip: EN low, VIN low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good (PG)

Output The VE2430Q includes an open-drain power good (PG) output that indicates whether the regulator output is within ±10% of its nominal output range. When the output voltage moves outside of this range, the PG output is pulled to ground.

APPLICATION

Setting the Output Voltage

Set the output voltage of the VE2430Q by using a resistor divider (see Figure 36.).

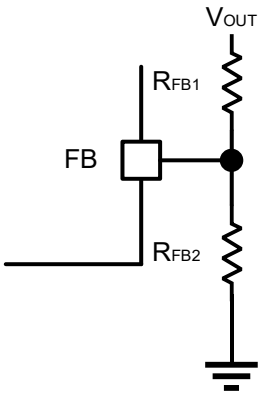


Figure 36. FB Resistor Divider to Set V_{OUT}

Choose R_{FB1} first, R_{FB2} can then be calculated with Equation (3):

$$R_{FB2} = R_{FB1} \div \left(\frac{V_{OUT}}{0.8V} - 1\right) \qquad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages. For fixed output version, connect FB pin to the output directly.

Table 1. Internal FB Resistor Divider

Fixed-Output Voltage	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3V	41.2	13

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can then be calculated with Equation (4):

$$L = \frac{V_{OUT}}{\Delta I_L \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (4)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (5):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2LF_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7μF to 10μF capacitor. It is strongly recommended to use another lower-value capacitor (e.g.: 0.1μF) with a small package size (0603) to absorb high frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since CIN absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple caused by the capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{F_{SW}C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$V_{RIPPLE} = \frac{V_{OUT}}{L \times F_{SW}} (1 - \frac{V_{OUT}}{V_{IN}}) (R_{ESR} + \frac{1}{8F_{SW} \times C_{OUT}}) \quad (9)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$V_{RIPPLE} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$V_{RIPPLE} = \frac{V_{OUT}}{F_{SW} \times L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The VE2430Q can be optimized for a wide range of capacitance and ESR values.

VIN UVLO Setting

The VE2430Q has an internal, fixed, UVLO threshold. The rising threshold is 2.8V, while the falling threshold is about 2.65V. For applications that require a higher UVLO point, an external resistor divider between VIN and EN can be used to achieve a higher equivalent UVLO threshold (see Figure 37.).

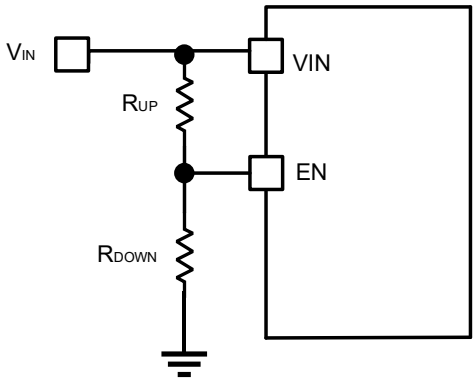


Figure 37. Adjustable UVLO Using EN Divider

The UVLO threshold can be calculated with Equation (12) and Equation (13):

$$INUV_{RISING} = \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \times V_{EN_{RISING}} \quad (12)$$

$$INUV_{FALLING} = \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \times V_{EN_{FALLING}} \quad (13)$$

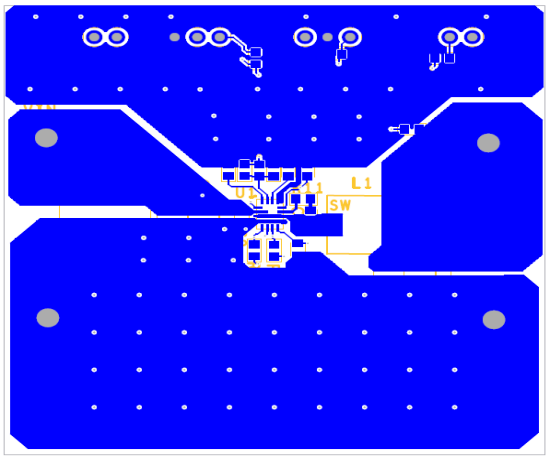
Where V_{EN_RISING} is 1.05V, and $V_{EN\_FALLING}$ is 0.93V.

PCB Layout Guidelines

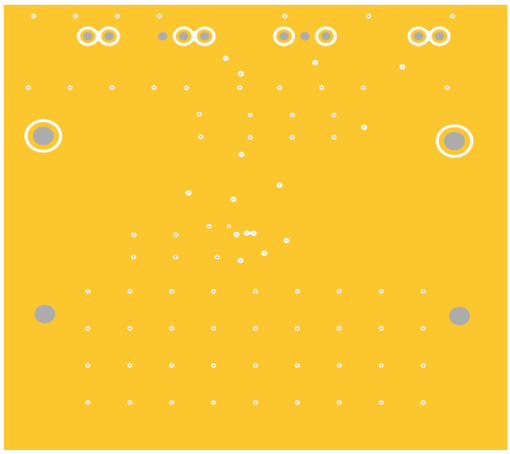
Efficient PCB layout, is critical for stable operation, especially for the input capacitor placement. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, follow the guidelines below:

1. Place the symmetric input capacitors as close to VIN and GND as possible. Recommend to connect pin1 to GND for symmetric input structure if in-phase not used. Pin3 and pin10 are internally connected. Connecting together on layout or not are both OK. Recommend to leave pin3 floating for shorter pin4 and pin1 trace and smaller input hot loop.
2. Use a large ground plane to connect to PGND directly.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitors, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high frequency noise.
6. Keep the connection of the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas such as FB.
9. Place the feedback resistors close to the chip to ensure that the trace connecting to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

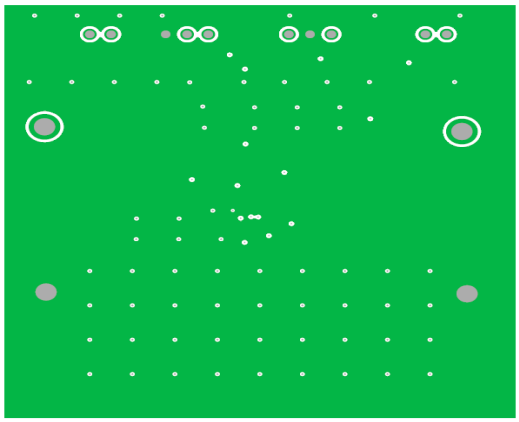
Top Layer



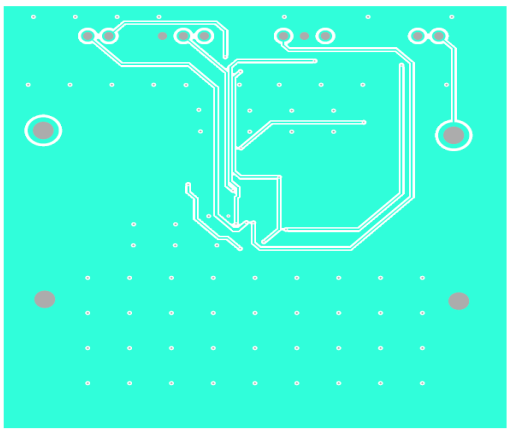
Bottom Layer



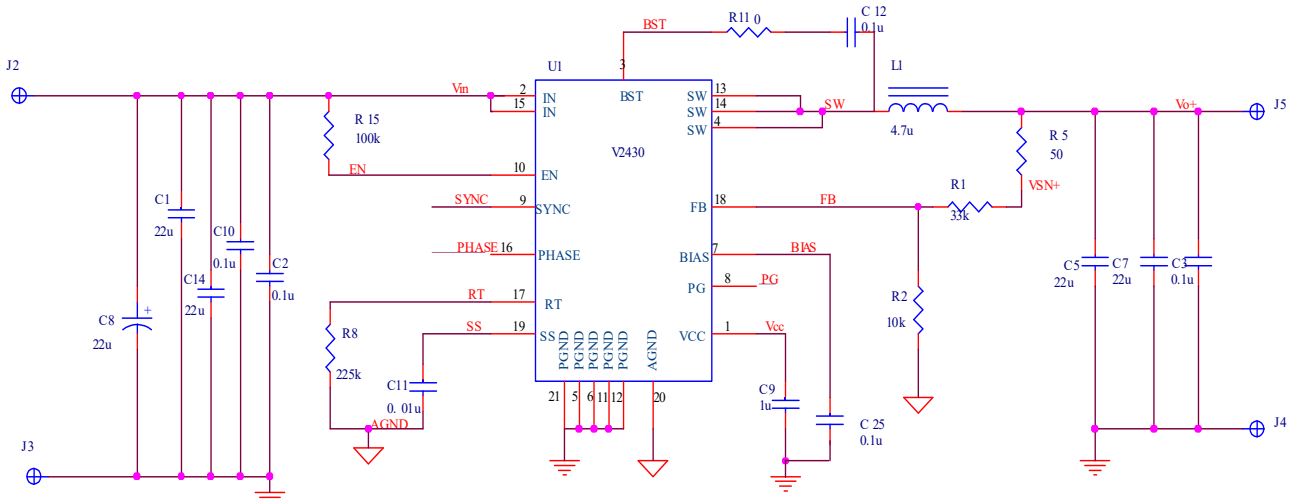
Inner Layer 1



Inner Layer 2



TYPICAL APPLICATION CIRCUITS

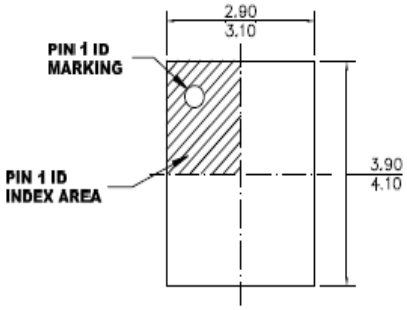


V_{IN}=12V, V_{OUT}=3.3V, L= 4.7uH, F_{SW}=500 kHz application

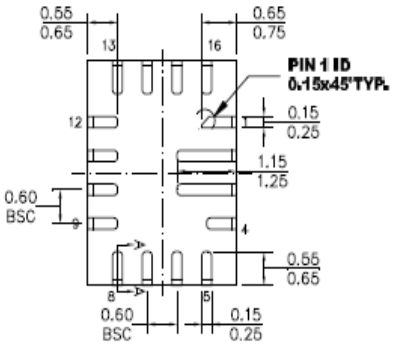
PACKAGE INFORMATION

FCQFN3X4-16（Wettable Flank）

QFN-16 (3mmx4mm)
Wettable Flank

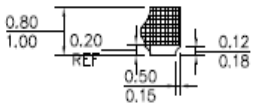


TOP VIEW

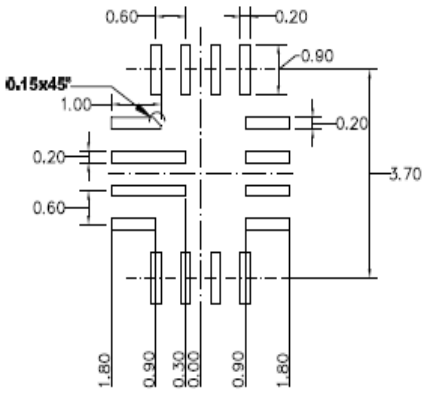


BOTTOM VIEW

SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision	Data	Description
1.0	2024-10-18	Initial Release