20V 20A Synchronous Step-Down Regulator

DESCRIPTION

The VE2220 is a high efficiency monolithic synchronous buck regulator capable of delivering 20A to the load. It uses a phase lockable controlled on-time constant frequency, current mode architecture. Multi-phase operation allows multiple VE2220 regulators to run out-of-phase, which reduces the amount of input and output capacitors required. The operating supply voltage range is from 3.3V to 20V. The operating frequency is programmable from 400kHz to 3MHz with an external resistor. The high frequency capability allows the use of physically smaller inductor and capacitor sizes. For switching noise sensitive applications, the VE2220 can be externally synchronized from 400kHz to 3MHz. The PHMODE pin allows the user control of the phase of the outgoing clock signal. The unique constant frequency/controlled on-time architecture is ideal for high step-down ratio applications that operate at high frequencies while demanding fast transient response. The VE2220 uses special low switching stress design including integrated bypass capacitors to deliver a highly efficient solution at high frequencies with excellent EMI performance.

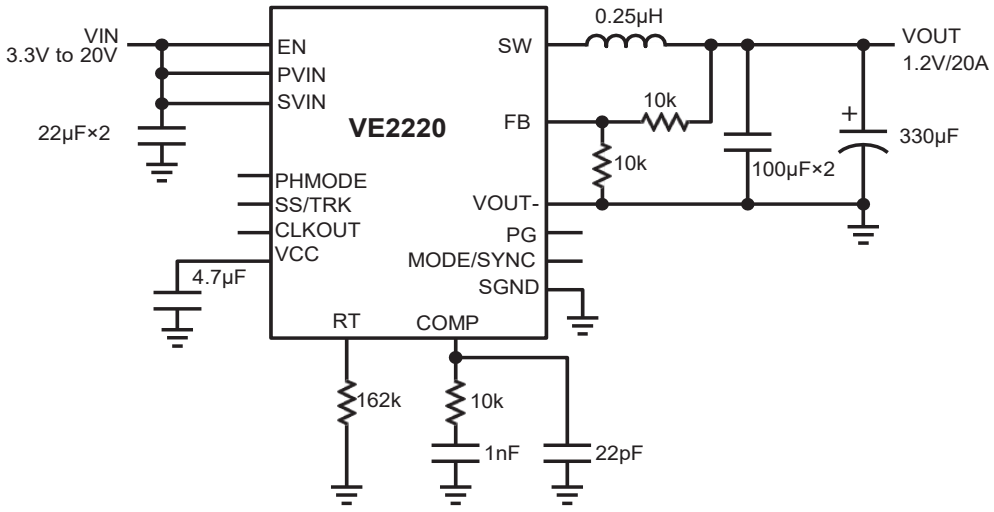
FEATURES

- Low EMI design
- V_{IN} Range: 3.3V to 20V
- V_{OUT} Range: 0.6V to 5.5V
- Differential V_{OUT} Remote Sense
- Adjustable Frequency: 400kHz to 3MHz
- Multi-phase Operation: Up to 12 Phases
- Output Tracking and Soft-Start
- Reference Accuracy: 0.6V ±1% Over Temperature
- Current Mode Operation for Excellent Line and Load Transient Response
- Accurate 1.2V EN Pin Threshold
- Supports Forced Continuous/Discontinuous Modes
- 42-Ball 6mm × 5mm × 1.3mm BGA Package

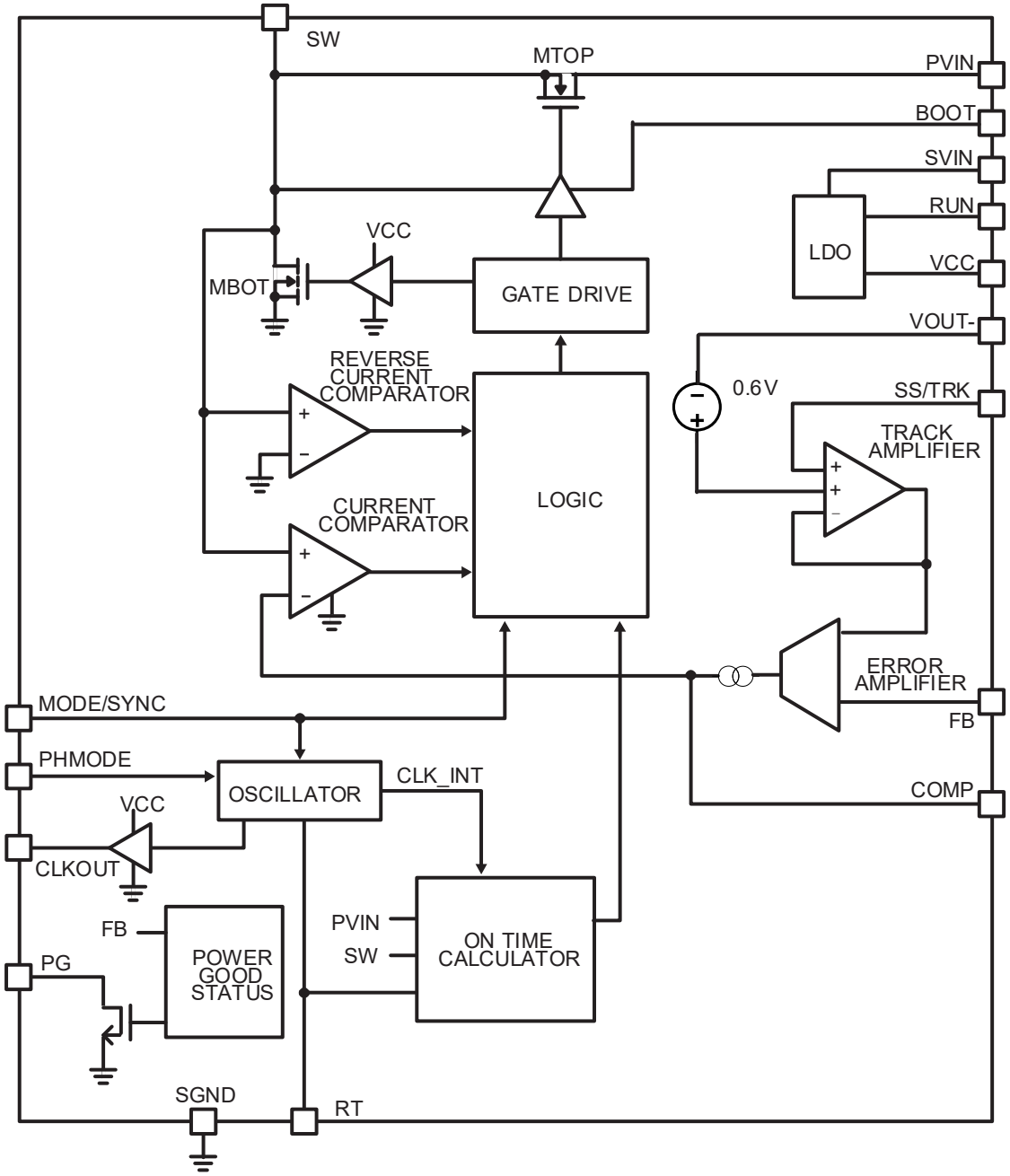
APPLICATIONS

- Industrial Application

TYPICAL APPLICATION



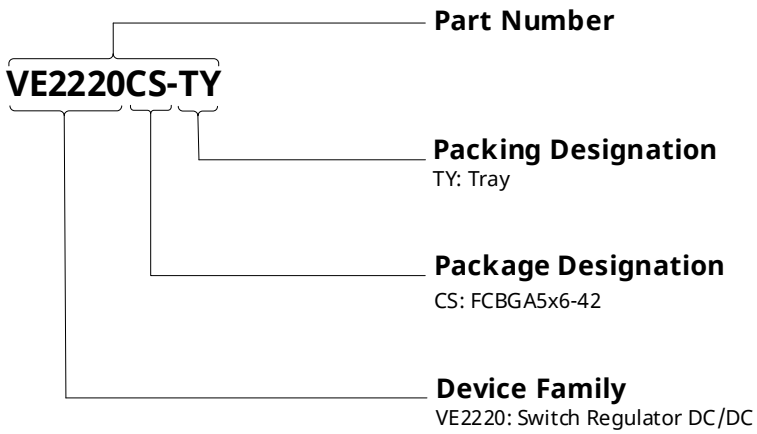
BLOCK DIAGRAM



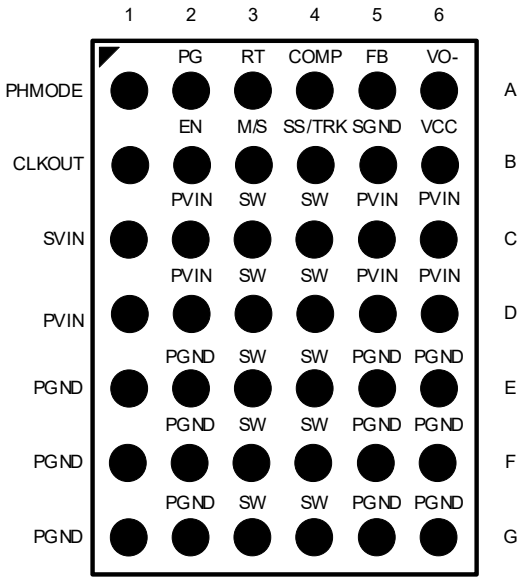
ORDERING INFORMATION

Ordering Information	Mark	Temperature Range	Package	Pack	Quantity
VE2220CS-TY	2220	-40 to +125°C	FCBGA5x6-42	TY	490
VE2220P(1)		-40 to +125°C			

Note 1: This product is available only in wafer form and is not offered in packaged versions.



PIN CONFIGURATIONS



BGA PACKAGE
42 Ball (6mmx5mmx1.3mm)

PIN DESCRIPTION

Name	FCBGA5X6-42	Description
PHMODE	A1	**Multi-phase Operation Mode.** Control Input to Phase Selector. Determines the phase relationship between internal oscillator and CLKOUT. Tie it to VCC for 2-phase operation, tie it to SGND for 3-phase operation, and tie it to VCC/2 (or float the pin) for 4-phase operation.
PG	A2	**Power Good Indicator.** Output Power Good with Open-Drain Logic. PG is pulled to ground when the voltage of the FB pin is not within ±8% of the internal 0.6V reference.
RT	A3	**Switching Frequency Programming Pin.** Connect an external resistor (between 405k to 54k) from this pin to GND to program the frequency from 400kHz to 3MHz.
COMP	A4	**Error Amplifier Output and Switching Regulator Compensation Point.** The current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 1.8V.
FB	A5	**Feedback Input to the Error Amplifier of the Step-Down Regulator.** Connect resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to V_{IN} by: V_{OUT} = 0.6V • [1 + (R1/R2)].
VOUT-	A6	**Negative Return of Output Rail.** Connect this pin directly to the bottom of the remote output capacitor near the load in order to minimize error incurred by voltage drop across the metal trace of the board.
CLKOUT	B1	**Output Clock Signal for Multi-Phase Operation.** The phase of CLKOUT with respect to CLKIN is determined by the state of the PHMODE pin. CLKOUT's peak-to-peak amplitude is VCC to GND.
EN	B2	**Logic Controlled EN Input.** Do not leave this pin floating. Logic High activates the step-down regulator.
MODE/SYNC	B3	**Discontinuous Mode Select and Oscillator Synchronization Pin.** Tie MODE/SYNC to GND for discontinuous mode of operation. Floating MODE/SYNC or tying it to a voltage above 1V will select forced continuous mode. Furthermore, connecting MODE/ SYNC to an external clock will synchronize the system clock to the external clock and puts the part in forced continuous mode.
SS/TRK	B4	**Output Tracking and Soft-Start Pin.** Allows the user to control the rise time of the output voltage. Putting a voltage between 0.6V on this pin relative to V_{OUT}– bypasses the internal reference input to the error amplifier, instead it servos the FB pin relative to V_{OUT}– to that voltage. There's an internal 5μA pull-up current from VCC to this pin, so putting a capacitor from this pin to V_{OUT}– provides a soft-start function.
SGND	B5	**Signal GND.**
VCC	B6	**Internal 3.3V Regulator Output.** The internal power drivers and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7μF low ESR ceramic capacitor.
SVIN	C1	**Signal VIN.** Filtered input voltage to the on-chip 3.3V regulator. Bypass signal into the SVIN pin with a 0.1μF ceramic capacitor.
PVIN	C2, C5,C6, D1, D2,D5, C6	**Power VIN.** Power this pin input voltage to the on chip power MOSFETS.
SW	C3, C4,D3, D4, E3, F3, F4, G3, G4	**Switch Node.** Connect an External Inductor from this pin to output capacitors. Voltage swing of SW is from a diode voltage drop below ground to a diode voltage above PVIN.
PGND	E1, E2, E5, E6, F1, F2, F5, F6, G1, G2, G5, G6	**Power Ground.**

ABSOLUTE MAXIMUM RATINGS

Parameter	Minimum	Maximum	Unit
PVIN, SVIN	-0.3	+22	V
EN Voltage	-0.3	SVIN	V
MODE/SYNC, SS/TRK Voltage	-0.3	VCC	V
COMP, RT, PG Voltage	-0.3	3.6	V
PHMODE, CLK Voltage	-0.3	3.6	V
VOUT- Voltage	-0.3	0.3	V
FB Voltage	-0.3	3.6	V
Storage Temperature	-65	+150	°C

ESD RATINGS

Parameter	Value	Unit
Human Body Model (HBM)	2	kV
Charged Device Model (CDM)	1250	V
Latch-Up	100	mA

THERMAL INFORMATION

Thermal Resistance	θ_{JA}(°C/W)
FCBGA5X6-42	21

RECOMMENDED OPERATINIG CONDITIONS

Parameter	Minimum	Maximum	Unit
VIN	3.3	20	V
VOUT	0.6	5.5	V
Operating Junction Temperature	-40	+125	°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
SVIN Operating Voltage	V_{SVIN}		●	3.3		20	V
PVIN Operating Voltage	V_{PVIN}					20	V
VOUT Operating Voltage	V_{OUT}			0.6		5.5	V
Input Quiescent Current (Note 3)	I_Q	Active Mode Shutdown Mode; VEN = 0V			2 20		mA uA
Feedback Reference Voltage (Note 4)	V_{FB}	COMP = 1.0V COMP = 1.0V, –40°C to 150°C	 ●		0.600 0.600		V V
Feedback Voltage Line Regulation	ΔV_{LINE_REG}	V_{IN} = 3.3V to 20V –40°C to 150°C	●			0.04	%/V
Feedback Voltage Load Regulation	ΔV_{LOAD_REG}	COMP = 0.5V to 1.5V –40°C to 150°C	●			0.2	%
Feedback Pin Input Current	I_{FB}				0		nA
Error Amplifier Transconductance	g_m(EA)	COMP = 1V			1.3		mS
Minimum On-Time	$T_{ON(MIN)}$		●		30		nS
Minimum Off-Time	$T_{OFF(MIN)}$				120		nS
Positive Inductor Valley Current Limit	I_{LIM}	FB = 0.58V	●		24		A
Current Limit at Different COMP Voltage	$I_{LIM-COMP}$	COMP = 1.4V COMP = 1V COMP = 0.6V COMP = 0.2V	● ● ● ●		12 0 –12 –24		A A A A
Top Power NMOS On-Resistance	R_{TOP}	V_{CC} = 3.3V			6		mΩ
Bottom Power NMOS On-Resistance	R_{BOT}	V_{CC} = 3.3V			2.5		mΩ
Top Switch Leakage Bottom Switch Leakage	I_{SW} (Note5)	VIN = 20V, SW = 0V VIN = 20V, SW = 20V				1 63	uA
V_{CC} Undervoltage Lockout Threshold	V_{UVLO}	V_{CC} Falling V_{CC} Hysteresis (Rising)			2.8 160		V mV
EN Rising EN Falling Hysteresis	V_{EN}				1.20 200		V mV
EN Leakage Current	I_{EN}					100	nA
Internal V_{CC} Voltage	V_{VCC}				3.3		V
Output Overvoltage PG Upper Threshold	OV	V_{FB} Rising V_{FB} Falling Hysteresis			8 10		% mV
Output Undervoltage PG Lower Threshold	UV	V_{FB} Falling V_{FB} Rising Hysteresis			-8 10		% mV
PG Pull-Down Resistance	R_{PG}	V_{PG}=100mV			4		Ω
PG Leakage	I_{PG}	V_{FB} = 0.6V				2	uA
PG Delay	T_{PG}	PG Low to High			6		cycles

Parameters	Symbol	Condition		Min	Typ	Max	Units
		PG High to Low			25		
Track Pull-Up Current	$I_{SS/TRK}$	$V_{SS/TRK}$ =0V			6		uA
Oscillator Frequency	F_{OSC}	RT = 162kΩ	●		1		MHz
SYNC Capture Range	F_{SYNC}	% of Programmed Frequency		70		110	%
MODE/SYNC Threshold Input High MODE/SYNC Threshold Input Low	MODE/ SYNC			0.3		1	V V
MODE/SYNC Current	$I_{MODE/SYNC}$	MODE/SYNC = 0V			6		uA
Clock Output High Voltage Clock Output Low Voltage	V_{CLKOUT}				V_{CC} 0		V V
PHMODE Threshold	PHMODE	180° (2-Phase)		V_{CC} -0.1			V
		90° (4-Phase)		1.0		V_{CC} -1	V
		120° (3-Phase)				0.1	V
VIN Overvoltage Threshold	V_{INOV}	VIN Rising VIN Falling			22.1 21.1		V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The VE2220 is tested under pulsed load conditions such that $T_J \approx T_A$. The VE2220 is guaranteed to meet specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The VE2220 is guaranteed over the –40°C to 150°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (PD, in Watts) according to the formula: $T_J = T_A + (PD \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: The quiescent current in forced continuous mode does not include switching loss of the power FETs.

Note 4: The VE2220 is tested in a feedback loop that servos VCOMP to a specified voltage and measures the resultant VFB.

Note 5: There is additional switch current due to internal resistor to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A=25℃, V_{IN}=12V, V_{OUT}=1.2V, Frequency = 400kHz, unless otherwise noted.

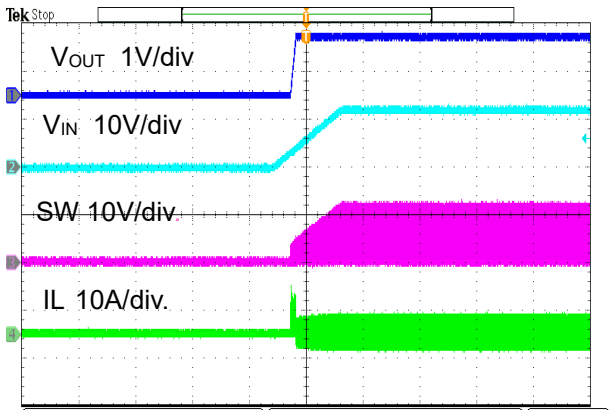


Figure 1. Vin Startup No Load

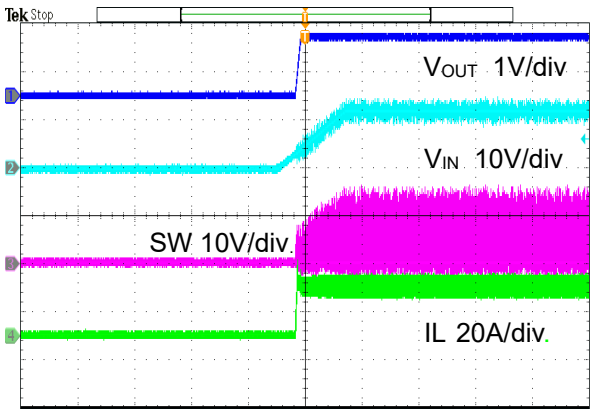


Figure 2. Vin Start-up Full Load

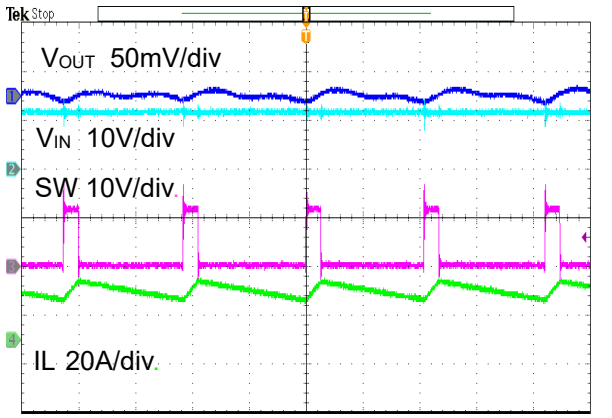


Figure 3. Output Ripple Full Load

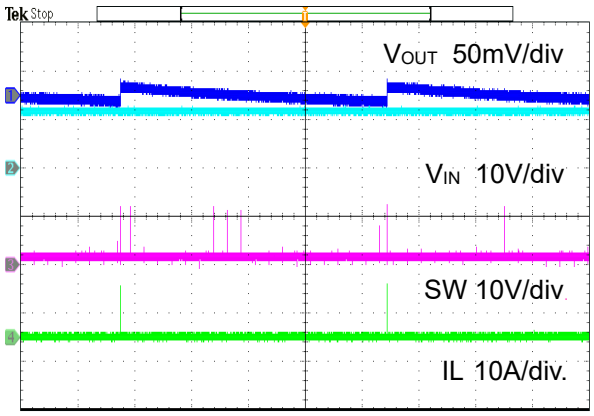


Figure 4. Output Ripple DCM No Load

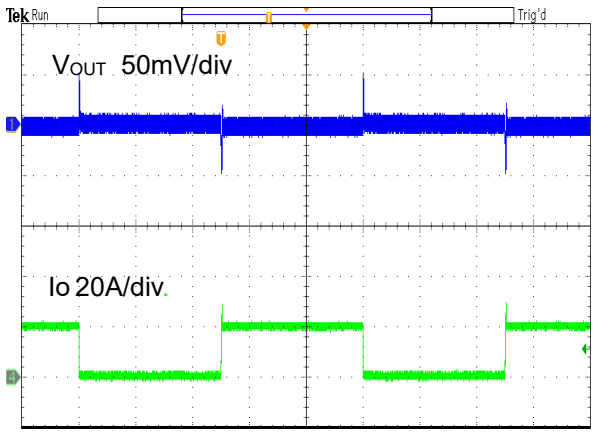


Figure 5. Load Transient 0-20A CCM

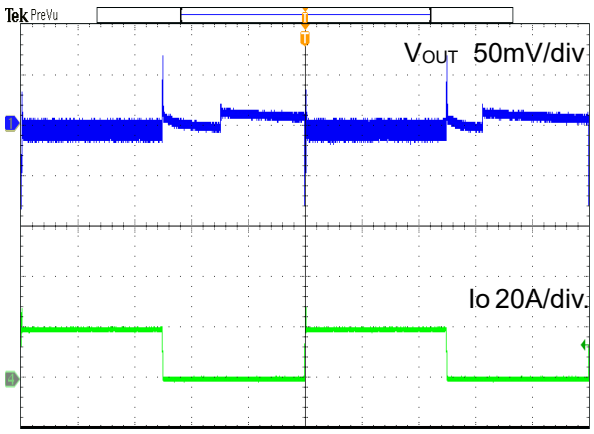


Figure 6. Load Transient 0-20A DCM

TYPICAL PERFORMANCE CHARACTERISTICS

T_A=25℃, V_{IN}=12V, V_{OUT}=1.2V, Frequency = 400kHz, unless otherwise noted.

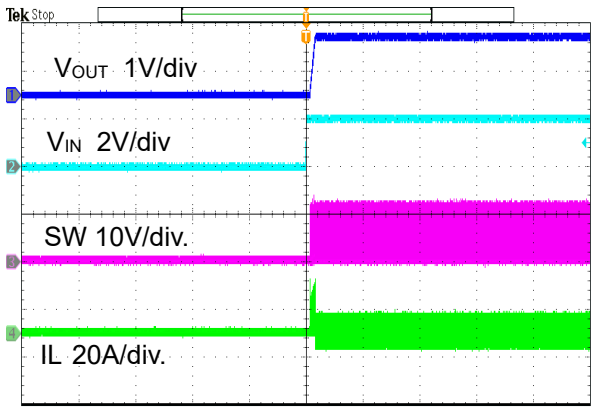


Figure 7. EN Startup No Load

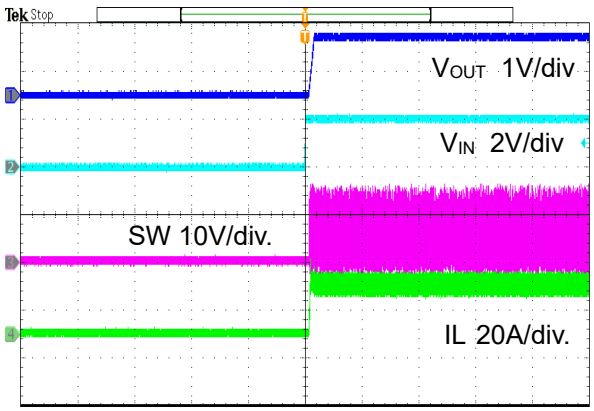


Figure 8. EN Startup Full Load

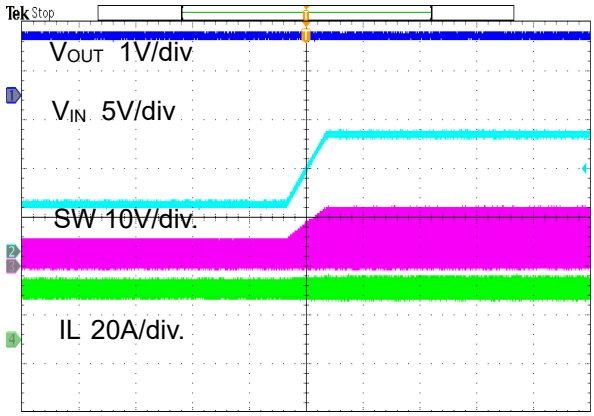


Figure 9. Line Transient 20A 5V->12V

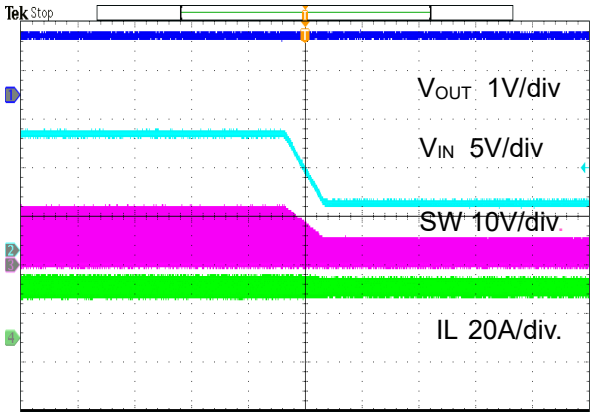


Figure 10. Line Transient 20A 12V->5V

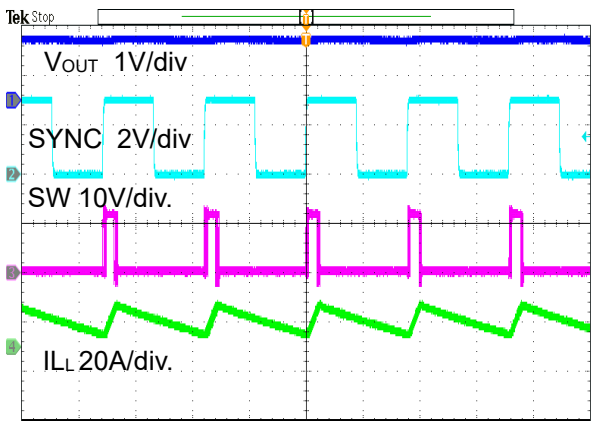


Figure 11. SYNC 280kHz Full Load

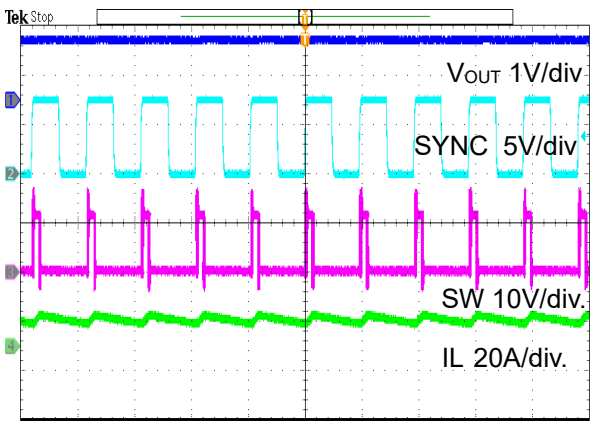


Figure 12. SYNC 520kHz Full Load

TYPICAL PERFORMANCE CHARACTERISTICS

T_A=25℃, V_{IN}=12V, V_{OUT}=1.2V, Frequency = 400kHz, unless otherwise noted.

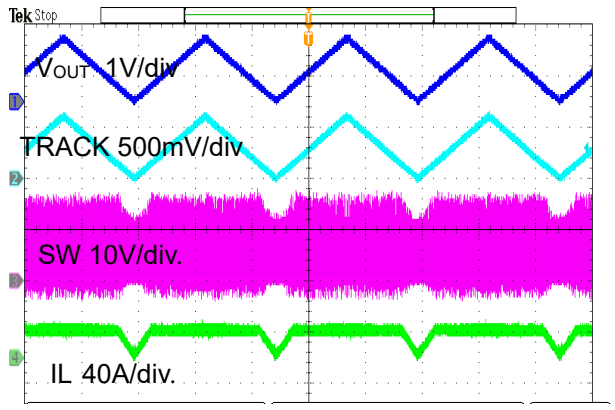


Figure 13. TRACK 0-600mV Full Load

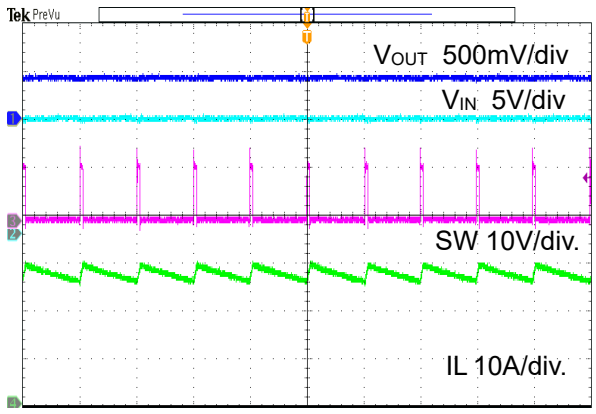


Figure 14. Short Circuit

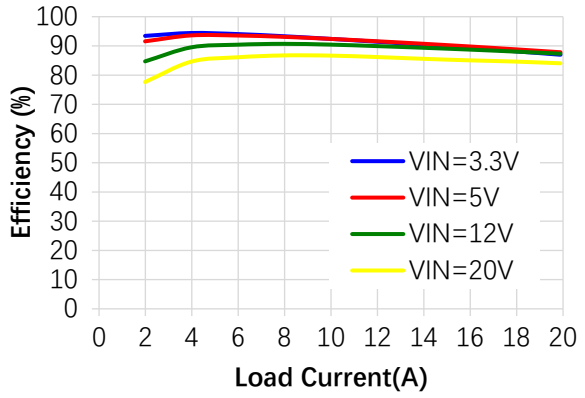


Figure 15. Efficiency Curve

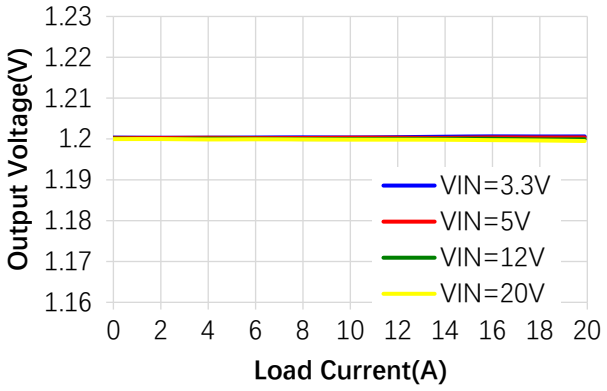


Figure 16. Load Regulation

FUNCTION DESCRIPTION

Main Control Loop

The VE2220 is a current mode monolithic 20A stepdown regulator. In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a one-shot timer, OST. When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator ICMP trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage drop across the bottom power MOSFET when it is on. The voltage on the COMP pin sets the comparator threshold corresponding to the inductor valley current. The error amplifier, EA, adjusts this COMP voltage by comparing the feedback signal, V_{FB}, with an internal 0.6V reference. If the load current increases, it causes a drop in the feedback voltage relative to the internal reference, the COMP voltage then rises until the average inductor current matches that of the load current.

At low load currents, the inductor current can drop to zero and become negative. In discontinuous mode (DCM), this is detected by the current reversal comparator, IREV, which then shuts off the bottom power MOSFET. Both power MOSFETs will remain off with the output capacitor supplying the load current until the COMP voltage rises above zero current level to initiate the next cycle. If continuous mode of operation is desired, simply float the MODE/SYNC pin or tie it to VCC.

The operating frequency is determined by the value of the RT resistor, which programs the current for the internal oscillator. An internal phase-lock loop servos the oscillator frequency to an external clock signal if one is present on the MODE/SYNC pin. Another internal phase-lock loop servos the switching regulator on-time to track the internal oscillator to force a constant switching frequency.

Overvoltage and undervoltage comparators OV and UV pull the PG output low if the output feedback voltage, VFB, exits a ±8% window around the regulation point. Continuous operation is forced during OV and UV conditions except during start-up when the TRACK pin is ramping up to 0.6V.

The VE2220 has some dedicated designs for EMI improvements. The IC has integrated ceramic capacitors for VIN and BOOT to keep all the fast AC current loops small, thus improving the EMI performance. Furthermore, it allows for faster switching edges which greatly improves efficiency at high switching frequencies.

EN Threshold

Pulling the EN pin to ground forces the VE2220 into its shutdown state. Bringing the EN pin to above 0.6V will turn on the internal reference only, while keeping the power MOSFETs off. Further increasing the EN voltage above the EN rising threshold (nominally 1.2V) turns on the entire chip. The accurate 1.2V EN threshold allows the user to program the SVIN under voltage lockout threshold by placing a resistor divider from SVIN.

VCC Regulator

An internal low dropout (LDO) regulator produces the 3.3V supply that powers the drivers and internal bias circuitry. The VCC must be bypassed to ground with a minimum of a 4.7μF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will experience an increase in die temperature due to the

higher power dissipation across the LDO. In such cases, if there's another 5V or 3.3V supply rail available, consider using that to drive the SVIN pin to lower the power dissipation across the internal LDO.

VIN Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the VE2220 constantly monitors the PVIN pin for an overvoltage condition. When the PVIN rises above 22.1V, the regulator suspends operation by shutting off both power MOSFETs. Once PVIN drops below 21.1V, the regulator immediately resumes normal operation. During an overvoltage event, the internal soft-start voltage is clamped to a voltage slightly higher than the feedback voltage, thus the soft-start feature will be present upon exiting an overvoltage condition.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.6V \cdot (1 + \frac{R1}{R2})$$

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 17. Since the VE2220 will often be used in high power applications, there can be significant voltage drop due to board layout between the part and the point of load (POL). Thus, it is imperative to have R2 and R1 Kelvin directly to the positive and negative terminals of the point of load. The negative terminal should then be connected directly to the V_{OUT}– pin of the VE2220 for differential V_{OUT} sensing. A feed forward compensation capacitor, C_{FF}, can also be placed between V_{OUT} and FB to improve transient performance.

In applications where the POL is far from the IC, it is a good idea to place a 0.1μF capacitor from V_{OUT}– to GND close to the IC to filter any noise that might be injected onto the V_{OUT}– trace.

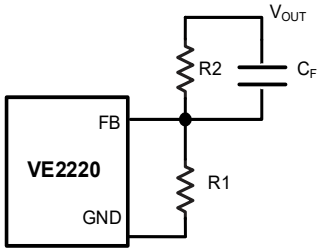


Figure 17. Setting the Output Voltage differentially

Programming Switching Frequency

Connecting a resistor from the RT pin to SGND programs the switching frequency from 400kHz to 3MHz according to the following formula:

$$\text{Frequency} = \frac{1.67 \cdot 10^{11}}{R_T(\Omega)}$$

The internal PLL has a synchronization range of ±30% around its programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this ±30% range of the RT programmed frequency. See plot of switching frequency vs RT value in the Typical Performance Characteristics section.

Output Voltage Tracking and Soft-Start

The VE2220 allows the user to program its output voltage ramp rate by means of the SS/TRK pin. An internal 6μA current pulls up the SS/TRK pin to VCC. Putting an external capacitor on SS/TRK enables soft starting the output to prevent current surge on the input supply. For output tracking applications, SS/TRK can be externally driven by another voltage source. From 0V to 0.6V, the SS/TRK voltage will override the internal 0.6V reference input to the error amplifier, thus regulating the feedback voltage to that of the SS/TRK pin. During this start-up time, the VE2220 will operate in discontinuous mode. When SS/TRK is above 0.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The relationship between output rise time and SS/TRK capacitance is given by:

$$T_{ss} = 120000 \cdot C_{SS/TRK}$$

A default internal soft-start ramp forces a minimum soft-start time of 100μs by overriding the SS/TRK pin input during this time period. Hence, capacitance values less than approximately 820pF will not significantly affect soft-start behavior.

Multiphase Operation

For output loads that demand more than 20A of current, multiple VE2220 can be paralleled to run out-of-phase to provide more output current. The MODE/SYNC pin allows the VE2220 to synchronize to an external clock and the internal phase-locked-loop allows the VE2220 to lock onto MODE/SYNC's phase as well. The CLKOUT signal can be connected to the MODE/SYNC pin of the following VE2220 to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to VCC, SGND or floating the pin generates a phase difference between the clock applied on the MODE/SYNC pin and CLKOUT of 180° degrees, 120° degrees, or 90° degrees respectively, which corresponds to 2-phase, 3-phase, or 4-phase operation. A total of 12 phases can be paralleled to run simultaneously out-of-phase with respect to each other by programming the PHMODE pin of each VE2220 to different voltage levels.

External COMP Compensation

External compensation is mandatory for proper operation of the VE2220. Proper COMP components should be selected for loop optimization. The compensation network is shown in Figure18.

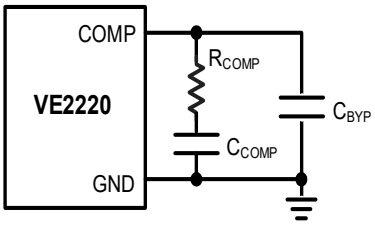


Figure 18. External Compensation Network

Table 1 provides a basic guideline for the compensation values that should be used given the frequency of the part. Slight tweaks to those values may be required depending on the amount of output capacitance used in the application.

Table 1. Compensation Values

Frequency	R_{COMP}	C_{COMP}	C_{BYP}
500kHz	4.99 kΩ	1.5nF	47pF
1MHz	10 kΩ	1nF	22pF
2MHz	15 kΩ	0.68nF	15pF
3MHz	20kΩ	0.47nF	10pF

Minimum Off-Time and Minimum On-Time Considerations

The minimum off-time, $T_{OFF(MIN)}$, is the smallest amount of time that the VE2220 is capable of turning on the bottom power MOSFET, tripping the current comparator and turning the power MOSFET back off. This time is generally about 50ns. The minimum off-time limit imposes a maximum duty cycle of T_{ON} /(T_{ON} + $T_{OFF(MIN)}$). If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \cdot \frac{T_{ON} + T_{OFF(MIN)}}{T_{ON}}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its “on” state. This time is typically 20ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of

$$DC_{MIN} = F_{SW} \cdot T_{ON(MIN)}$$

Where $T_{ON(MIN)}$ is the minimum on-time. Reducing the operating frequency will alleviate the minimum duty cycle constraint.

In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, and the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance in most cases. High switching frequencies may be used in the design without any fear of output overvoltage. As the sections on inductors and capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the size of the application circuit.

APPLICATION

Input Capacitor (C_{IN}) Selection

The input capacitance, C_{IN}, is needed to filter the square wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where

$$I_{RMS} \cong \frac{I_{OUT}}{2}$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8 \cdot F_{SW} \cdot C_{OUT}} + ESR \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the VIN input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size. Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. Typically, 5 cycles are required to respond to a load step, but only in the first cycle does the output voltage drop linearly. The output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately:

$$C_{OUT} = 3\frac{\Delta I_{OUT}}{F_{OUT} \cdot V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 47μF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the PVIN pin as possible.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \cdot L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

Table 2. Inductor Selection Table (Examples)

Vendor	Part Number	Inductance	Current(max)	Resistance	Dimensions	Height
		(nH)	(A)	(mΩ)	(mm)	(mm)
Wurth	744308015	150	25	0.37	10x7	6.8
	744308033	330	25	0.37	10x7	6.8
TDK	VLB10050HT-R15M	150	31	0.35	9.8X6.7	4.8
	VLB12065HT-R36M	360	27	0.44	11.6x9.7	6.3

A reasonable starting point is to choose a ripple current that is about 50% of $I_{OUT(MAX)}$. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{F_{SW} \cdot \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from TDK, Wurth Elektronik and Sunlord. Refer to Table 2 for more details.

Checking Transient Response

The loop compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the COMP pin not only allows for optimization of the control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects this close loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The COMP external component shown in the table 1 circuit will provide an adequate starting point for most applications. The RC filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested value) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1μs to 10μs will produce output voltage and COMP pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to the ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with the R_{COMP} and the bandwidth of the loop increases with decreasing C_{COMP}. If R_{COMP} is increased by the same factor that C_{COMP} is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in most critical frequency ranges of the feedback loop.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to loop design application notes.

In some applications, a more severe transient can be caused by switching in loads with large (>47μF) input capacitors. The discharge input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A unique controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in VE2220 circuits: 1) I^2R losses, 2) switching and biasing losses, 3) other losses.

1.I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is “chopped” between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I2R losses:

$$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

2.The switching current is the sum of the MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from IN to ground. The resulting dQ/dt is a current out of IN that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. The power loss is thus:

$$\text{Switching Loss} = I_{GATECHG} \cdot V_{IN}$$

The gate charge loss shows up as current through the VCC LDO and becomes larger as frequency increases. Thus, their effects will be more pronounced in applications with higher input voltage and higher frequency.

3. Other “hidden” losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these “system” level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The VE2220 internal power devices switch quickly enough that these losses are not significant compared to other sources. Other losses including diode conduction losses during dead-time and inductor core losses which generally account for less than 2% total additional loss.

Thermal Considerations

In some applications where the VE2220 is operated at a combination of high ambient temperature, high switching frequency, high VIN, and high output load, the required power dissipation might push the part to exceed its maxi-mum junction temperature. If the junction temperature reaches approximately 175°C, both power switches will be turned off until the temperature returns to 165°C.

To avoid the VE2220 from exceeding the maximum junction temperature, maximum current rating shall be derated depending on the operating conditions. The temperature rise of the part will vary depending on the thickness of copper on the PCB board, the number of layers of the board, and the shape of copper trace. In general, a thick continuous piece of copper on the top layer of the PCB for SW and GND pins will greatly improve the thermal performance of the part.

Reduce Power FET Stress

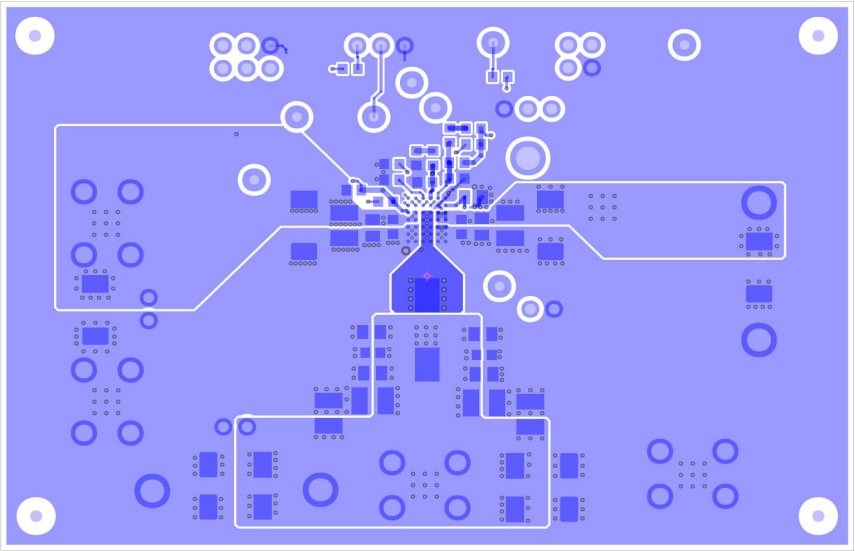
The VE2220 has integrated capacitors that allow it to operate at high switching frequencies efficiently. The internal VIN bypass capacitors allow the SW edges to transition extremely fast, effectively reducing transition loss. The capacitors also greatly reduce SW overshoot during top FET turn-on which improves the robustness of the device over time.

LAYOUT GUIDELINES

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the VE2220. Check the following in your layout:

1. Are there pairs of capacitors (C_{IN}) between VIN and GND as close as possible on both sides of the package? These capacitors provide the AC current to the internal power MOSFETs and their drivers as well as minimize EUI/EMC emissions.
2. Are C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.
3. Place the FB dividers close to the part with Kelvin connections to V_{OUT} and V_{OUT-} at the point of load, for differential V_{OUT} sensing.
4. Keep sensitive components away from the SW pin. The FB resistors, RT resistor, the compensation component, and the VCC bypass caps should be routed away from the SW trace and the inductor.
5. A ground plane is preferred.
6. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to GND.

Top Layer



Design Example

As a design example, consider the VE2220 in an application with the following specifications:

VIN = 12V to 15V

VOUT = 1.2V

IOUT(MAX) = 20A

IOUT(MIN) = 1A

F_{SW} = 1MHz

First, R_{FB1} and R_{FB2} should be the same value in order to program the output to 1.2V. A typical value that can be used here for both resistors is 10kΩ. For best accuracy, a 0.1% resistor should be used.

For a typical soft start time of 2ms (0% to 100% of final V_{OUT} value), the $C_{SS/TRK}$ should be:

$$6\mu A = C_{SS/TRK} \cdot \frac{0.6V}{2ms}$$

$$C_{SS/TRK} = 20nF$$

A typical 22nF capacitor can be used for $C_{SS/TRK}$.

Because efficiency is important at both high and low load current, discontinuous mode operation will be utilized. Select from the characteristic curves the correct RT resistor for the 1MHz switching frequency. Based on that, RT should be 162kΩ. Then calculate the inductor value to achieve a current ripple that is about 40% of the maximum output current (20A) at maximum VIN:

$$L = \left(\frac{1.2V}{1MHz \cdot 8A}\right)\left(1 - \frac{1.2V}{15V}\right) = 0.138\mu H$$

The closest standard value inductor higher would be 0.15μH.

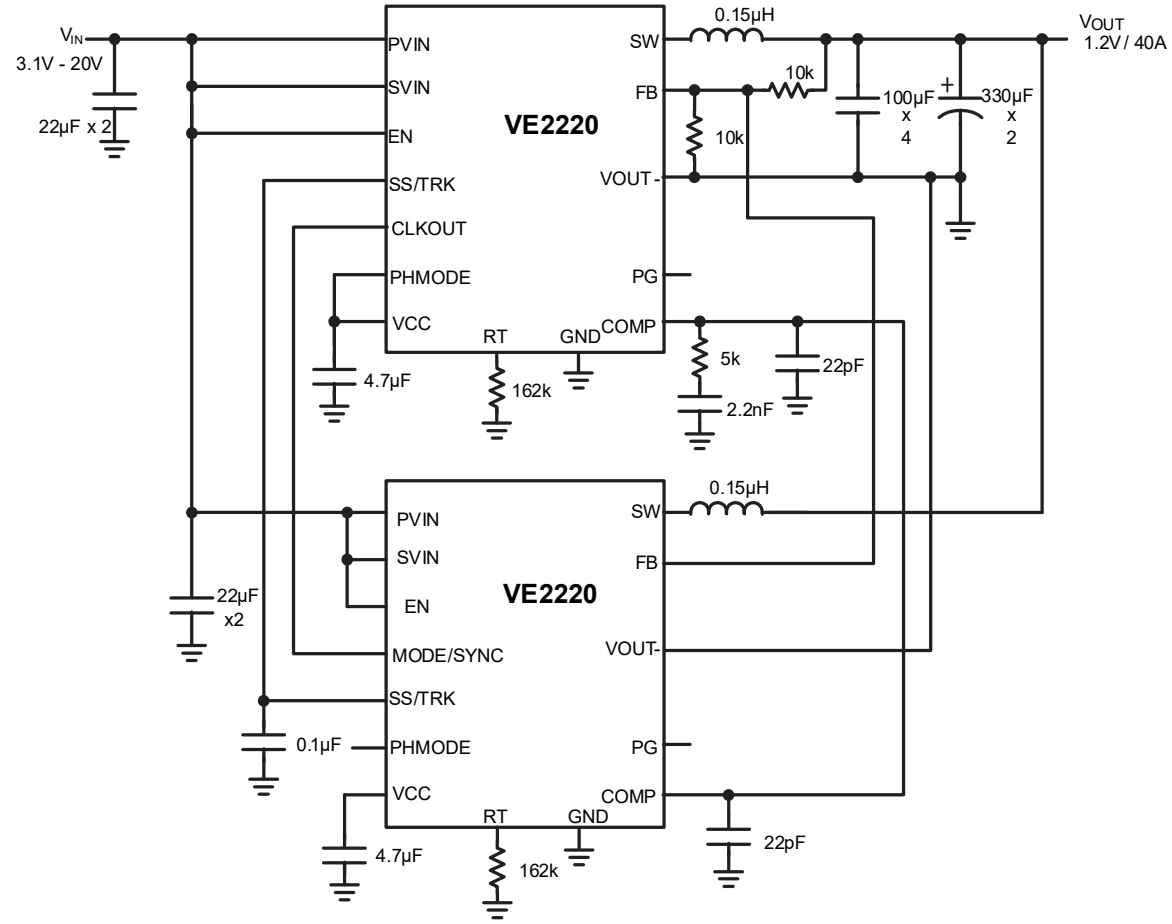
C_{OUT} will be selected based on the ESR that is required to satisfy the output ripple requirement and the bulk capacitance needed for loop stability. For this design, two 100μF ceramic capacitors will be used.

C_{IN} should be sized for a maximum current rating of:

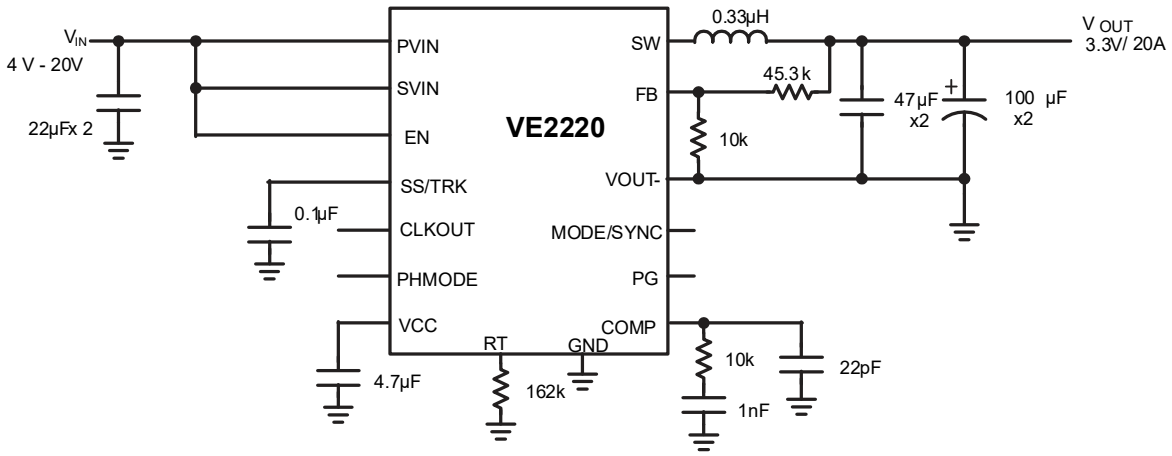
$$I_{RMS} = 20A\left(\frac{1.2V}{15V}\right)\left(\frac{15V}{1.2V} - 1\right)^{1/2} = 5.4A$$

Decoupling VIN with two 22μF ceramic capacitors, as shown in Figure 11, is adequate for most applications

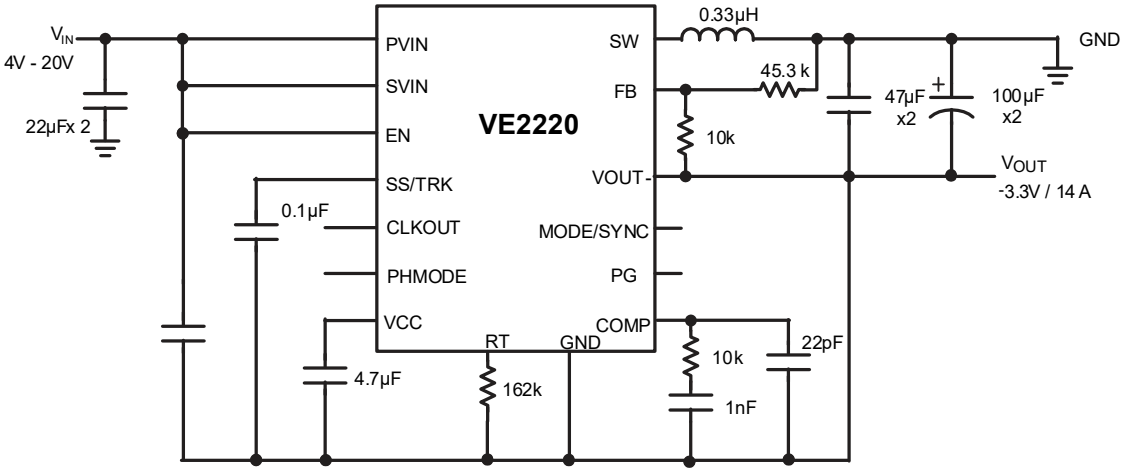
TYPICAL APPLICATION CIRCUITS



High Efficiency, Dual Phase 1.2V/40A Step-Down Supply application



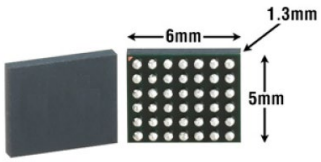
3.3V/20A Step-Down Converter application



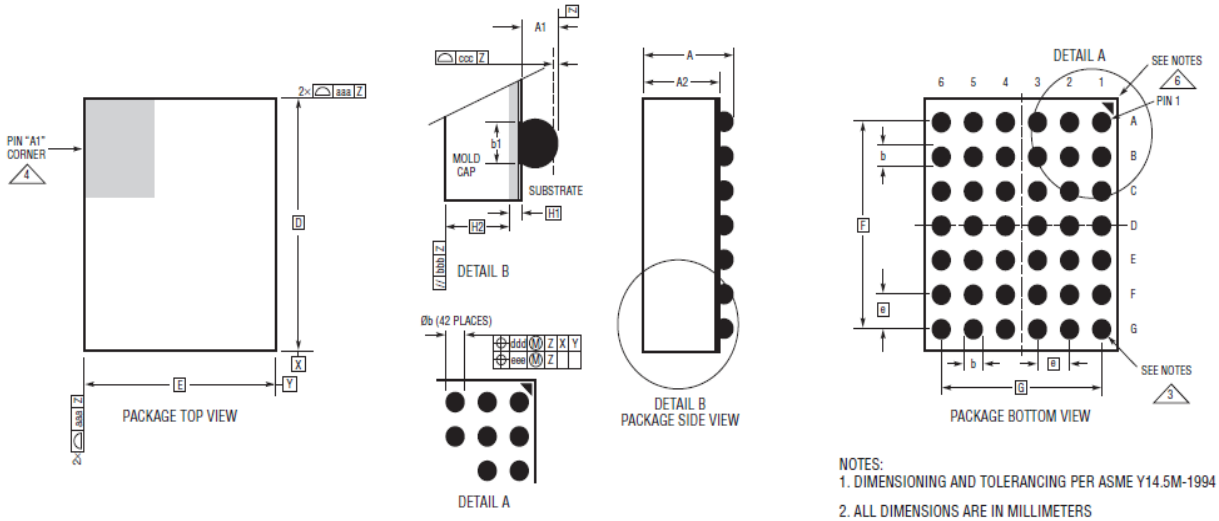
–3.3V_{OUT}, 14A Step-Down Converter application

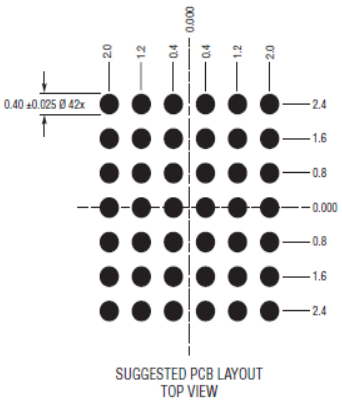
PACKAGE INFORMATION

FCBGA5X6-42



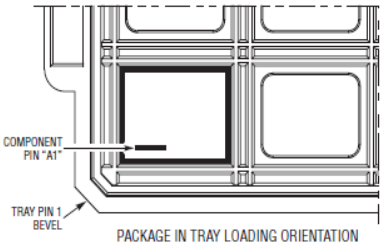
BGA Package 42-Ball (6mm × 5mm × 1.30mm)





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.10	1.30	1.50	
A1	0.30	0.40	0.50	BALL HT
A2	0.80	0.90	1.00	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		6.00		
E		5.00		
e		0.80		
F		4.80		
G		4.00		
H1		0.20		SUBSTRATE THK
H2		0.70		MOLD CAP HT
aaa			0.15	
bbb			0.20	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 42				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



REVISION HISTORY

Revision	Data	Description
1.0	2024-10-18	Initial Release