16-Bit High-Speed Inductive Position Sensor Chip Series

1. Features

- 16-bit resolution inductive position sensor IC
- Accuracy ≤ ±0.36° electrical angle, up to ≤ 0.05°
- Supports maximum rotational speed exceeding 600K rpm
- Auto-calibration function supported
- Supports multiple output interface options:
  - ABZ+PWM(SC60414)
  - SPI(SC60418)
- User configurable via SPI or single-wire programming interface
- Full diagnostic functions: open wire, short circuit, overvoltage, overtemperature, overcurrent, coil open circuit
- High reliability design: supply voltage withstand 48 V, output withstand 24 V
- Suitable for compact through-shaft mounting structure
- Strong electromagnetic interference immunity
- Operating temperature range: -40 ℃ to 150 ℃
- Package: miniature TSSOP-16, QFN 3×3-16

2. Applications

- Robotic joint control
- Main drive motor
- EPS motor
- Angular position for automotive applications
- E-Motorcycle brushless DC motor (BLDC Motor)

3. Description

SC6041X is a family of non-contact, high-speed, high-precision inductive position sensor ICs for high-speed absolute position sensing in automotive and industrial applications.

Based on the eddy current effect, the IC achieves accurate position measurement by detecting induced voltage variations caused by the displacement of a metal target above a set of coils.

SC6041X supports fine-tuning of output signals via programming pins after auto-calibration. With single-cycle coil design, it supports rotation speeds over 600K rpm, ultra-low propagation delay (< 4 μs), and near-zero delay under steady-state motor operation.

SC60414 provides incremental output through A, B, Z pins, supporting multiple line configurations up to 2048 lines, and outputs absolute position signals via the PWM pin.

SC60418 provides 16-bit resolution protocol output, allowing users to read internal 16-bit data through the interface.

SC6041X is offered in 16-pin TSSOP-16 and QFN 3×3-16 packages, featuring matte tin plating and halogen-free green molding compound for environmental compliance.

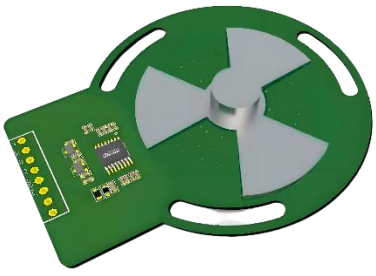

Fig.1 Schematic diagram of the work

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4. Pin Description

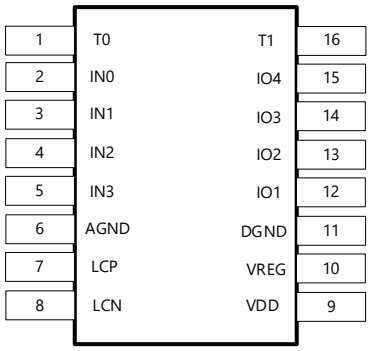


Fig.2 TSSOP16 Pin Description

Pin		Type	Pin function description
Name	No.		
T0	1	Output	Test pin
IN0	2	Input	Receiver coil input 0
IN1	3	Input	Receiver coil input 1
IN2	4	Input	Receiver coil input 2
IN3	5	Input	Receiver coil input 3
AGND	6	Ground	Analog ground
LCP	7	Input	Exciter coil positive output
LCN	8	Input	Exciter coil negative output
VDD	9	Power	Supply voltage
VREG	10	Output	Internal high-voltage LDO output; external 100 nF decoupling capacitor
DGND	11	Ground	Digital ground
IO1	12	I/O	SPI: CSn / Channel A incremental output
IO2	13	I/O	SPI: SCLK / Channel B incremental output
IO3	14	I/O	SPI: MOSI / Channel Z incremental output
IO4	15	Output	SPI: MISO / PWM absolute angle output
T1	16	I/O	Single-wire programming pin

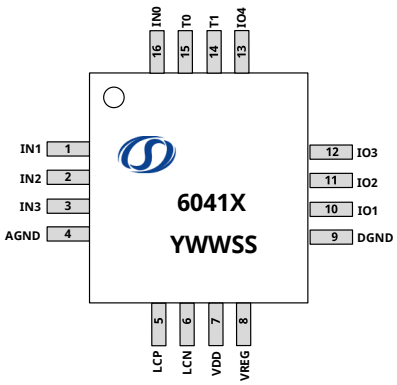


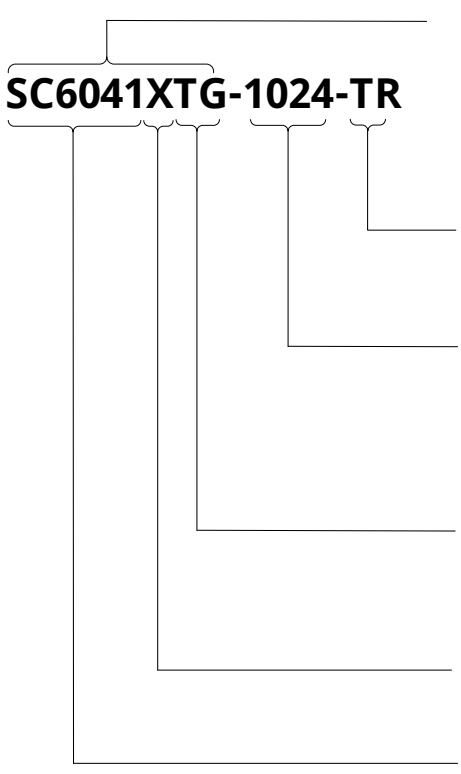
Fig.3 QFN3*3-16 Pin Description

Pin		Type	Pin function description
Name	No.		
IN1	1	Input	Receiver coil input 1
IN2	2	Input	Receiver coil input 2
IN3	3	Input	Receiver coil input 3
AGND	4	Ground	Analog ground
LCP	5	Input	Exciter coil positive output
LCN	6	Input	Exciter coil negative output
VDD	7	Power	Supply voltage
VREG	8	Output	Internal high-voltage LDO output; external 100 nF decoupling capacitor
DGND	9	Ground	Digital ground
IO1	10	I/O	SPI: CSn / Channel A incremental output
IO2	11	I/O	SPI: SCLK / Channel B incremental output
IO3	12	I/O	SPI: MOSI / Channel Z incremental output
IO4	13	Output	SPI: MISO / PWM absolute angle output
T1	14	I/O	Single-wire programming pin
T0	15	I/O	Test pin
IN0	16	Input	Receiver coil input 0

5. Ordering Information

Ordering Information	Mark	Output	Option	Ambient(℃)	Package	Pack	Amount
SC60414TG-1024-TR	60414	ABZ+PWM	1024	-40~150	TSSOP16	Tape&Reel	4000Pcs/Reel
SC60414QC-1024-TR	60414	ABZ+PWM	1024	-40~150	QFN3*3-16	Tape&Reel	5000 Pcs/Reel
SC60414TG-256-TR	60414	ABZ+PWM	256	-40~150	TSSOP16	Tape&Reel	4000Pcs/Reel
SC60414TG-50-TR	60414	ABZ+PWM	50	-40~150	TSSOP16	Tape&Reel	4000Pcs/Reel
SC60418TG-TR	60418	SPI	-	-40~150	TSSOP16	Tape&Reel	4000Pcs/Reel
SC60418QC-TR	60418	SPI	-	-40~150	QFN3*3-16	Tape&Reel	5000 Pcs/Reel

Ordering Information Format



Part Number

Package Options
TR: Tape & Reel

Parameter Options
1024=1024 lines
256=256 lines
50=50 lines

Package Designation
TG: TSSOP16
QC: QFN3*3-16

Output Form
4: ABZ+PWM
8: SPI

Device Family
SC6041X: High-speed inductive position sensor IC

6. Absolute Maximum Ratings

Full operating temperature range unless otherwise specified(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply voltage withstand	t < 60 s	-5.5	48	V
V_{REG}	Regulator output withstand	t < 60 s	-0.3	5.5	V
V_{IO}	Output withstand	-	-12	24	V
$V_{LCP/LCN}$	Exciter coil input	-	-0.5	5.5	V
V_{INX}	Receiver coil input	-	-0.5	5.5	V
SDA	Digital I/O	-	-0.5	5.5	V
SCL	Digital clock input	-	-0.5	5.5	V
T_A	Operating temperature	-	-40	150	℃
T_J	Junction temperature	-	-55	165	℃
T_{STG}	Storage temperature	-	-65	175	℃

Note:
(1)Stresses above those listed here may cause permanent damage to the device. Prolonged exposure to absolute maximum ratings may affect the reliability of the device.

7. ESD Protection

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{ESD_HBM}	HBM	Human failure model, refer to AEC-Q100-002 standard	-4	4	kV
V_{ESD_CDM}	CDM	Device failure model, refer to AEC-Q100-011 standard	-750	750	V

8. Operating Characteristics

Condition: unless otherwise specified, V_{DD} = 5V ±10%, T_A = -40°C to 160°C (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply Characteristics						
V_{DD_5v}	5V Application operating voltage	Refer to 5V application circuit connection	4.5	5.0	5.5	V
$V_{DD\_3.3v}$	3.3V Application operating voltage	Refer to 3.3V application circuit connection	3.0	3.3	3.6	V
I_{DD_5V}	5V Application operating current	V_{DD} = 5.0V	-	8.0	12	mA
$I_{DD\_3.3V}$	3.3V Application operating current	V_{DD} = 3.3V	-	7.0	11	mA
V_{VREG}	5V Operation, VREG pin voltage	V_{DD} = 5.0V	3.7	4.2	4.3	V
C_{VREG}	VREG pin decoupling capacitor		47	100	470	nF
V_{OVP}	Overvoltage detection threshold	Outputs disabled when supply voltage exceeds this threshold	6.5	7.0	7.5	V
V_{OVP_HYS}	Overvoltage detection hysteresis		0.2	0.5	0.8	V
V_{UVR}	Undervoltage detection threshold	Outputs disabled when supply voltage falls below this	3.4	3.7	4.3	V
V_{UVR_HYS}	Undervoltage detection hysteresis		0.1	0.3	0.5	V
LC oscillator characteristics						
I_{OSC}	LC oscillator drive current	L=3μH，C=1nF，Rs=2Ω	2.0	-	10	mA
V_{OSC}	LC oscillator oscillation amplitude	L=3μH，C=1nF，Rs=2Ω	3.0	3.5	4.0	Vpp
F_{OSC}	LC oscillator oscillation frequency	L=3μH，C=1nF，Rs=2Ω	2	4	5	MHz
L_{OSC}	Excitation coil inductance		2	-	10	μH
Coil input signals						
V_{PPIN}	IN_X input signal amplitude		5	-	100	mV

Operating Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
A/D Conversion Characteristics						
$R_{ES(SD)}$	ADC resolution		-	14	-	Bit
$T_{(ON)}$	Startup time		-	-	5	ms
ABZ/PWM Output Characteristics						
F_{PWM}	PWM frequency (Default)		927	976	1024	Hz
$F_{PWM(OPT)}$	PWM frequency (optional)		232	244	256	Hz
D_{UTY}	AB output duty cycle	Spinning at a constant speed of 1000 rpm	40	50	60	%
$R_{ES(AB)}$	Number of AB output lines		12	-	1024	RES
Z_{WIDTH}	Z zero position width		-	4	-	LSB
Rpm	Rotation speed	Single-turn coil	-	-	600000	rpm
Digital I/O Port Electrical Characteristics						
V_{THI}	Enter high-level threshold		-	-	2.0	V
V_{TLO}	Enter low voltage threshold		0.8	-	-	V
V_{SHI}	Output high-level voltage	4mA pull-down current	V_{DD}-0.5	-	-	V
V_{SLO}	Output low-level voltage	4mA pull-up current	-	-	0.5	V
V_{IH}	Input high level		0.5*V_{DD}	-	-	V
V_{OL}	Input low level		-	-	0.2*V_{DD}	V
V_{OH}	Output high level		0.8*V_{DD}	-	-	V
I_{SHI}	Output high-level short-circuit to ground current	V_{DD}=3.3V	-	-	30	mA
I_{SLO}	Output low-level short circuit to supply current	V_{DD}=3.3V	-	-	30	mA
Diagnostic Function						
Dsat_lo	Active diagnostic output level	Pull-down R≥4.7kΩ	-	0.5	1	%VDD
		Pull-up R≥4.7kΩ	99	99.5	-	%VDD
$BV_{SS}PD$	Passive diagnostic output level (open circuit)	VSS open circuit, pull-down resistor, 4.7kΩ≤R≤47kΩ	-	0	3	%VDD
$BV_{SS}PU$		VSS open circuit, pull-up resistor, 4.7kΩ≤R≤47kΩ	97	98	-	%VDD
$BV_{DD}PD$		VDD open circuit, pull-down resistor, 4.7kΩ≤R≤47kΩ	-	0	1	%VDD
$BV_{DD}PU$		VDD open circuit, pull-up resistor, 4.7kΩ≤R≤47kΩ	96.5	98	-	%VDD
OTP	Over-temperature protection		-	175	-	℃
$I_{\_OCP}$	Over current protection		-		30	mA

9. Functional Module

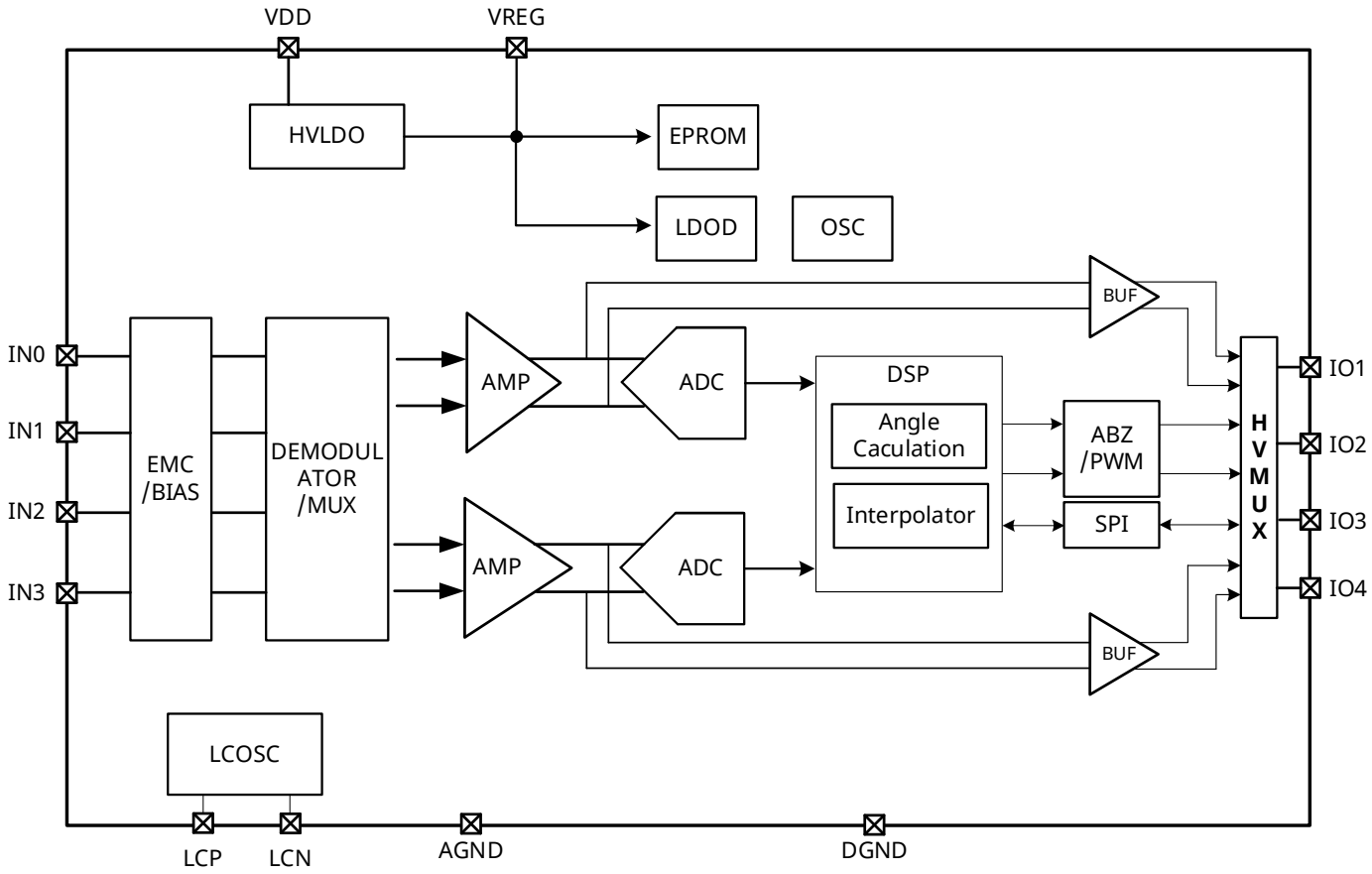


Fig.4 Functional Block Diagram

10. Functional Description

10.1. Auto-Calibration

External Trigger:

1、 With the external rotor in uniform rotation at a speed ≤ 600K rpm (Rotation speed affects auto-calibration completion time. For 1 kHz, the completion time is 2 s);

2、 After power-on, the device internally detects the voltage on output pins within 500 μs. When the output pins OUT1~OUT4 correspond to the status pattern '1001' (SIN+ and COS- connected to supply via 47 kΩ, SIN- and COS+ connected to ground via 47 kΩ), the auto-calibration mode is triggered;

3、 Internally processes the received signals, identifying the peak-to-peak amplitude and common-mode deviation after ADC conversion;

4、 By comparing with target values, internal feedback adjusts the signal gain and VOS compensation to bring the received signals within the target threshold range;

5、 Auto-calibration completes when both signal channels are within the target threshold range. The current gain and VOS compensation values are automatically programmed into the EEPROM, and a completion flag is issued, resulting in an additional 10 mA of device current consumption;

6、 If the internal gain or VOS compensation reaches its limit before the received signals are adjusted within the target threshold range, the optimal values are programmed into the EEPROM, and a completion flag is issued, resulting in an additional 10 mA of device current consumption. (The extra current is disabled after a power reset and does not affect normal operation. The 10 mA indicates that auto-calibration has completed. To determine whether auto-calibration was successful, query the status of the dedicated internal register via communication);

Active Programming Trigger:

1、After device power-on, initiate active programming by sending the designated code to enter auto-calibration mode;

Steps 2 through 6 are identical to those for external trigger operation.

10.2. Diagnostic Function

SC6041X integrates comprehensive self-diagnostic functions (safety mechanisms). These mechanisms enhance the safety of the entire sensor system by preventing random hardware faults in the connected inductive sensor that could cause incorrect output signals. Only sensor-event related monitoring items are listed in the table below. For a complete overview of safety mechanisms and monitoring, refer to the safety manual.

No.	Safety Mechanism	Output State (IO1、IO2、IO3、IO4)
1	Supply overvoltage protection	High-Z
2	Supply undervoltage protection	High-Z
3	Overcurrent protection	Current limit
4	Supply or GND pin open detection	High-Z
5	Inductive coil open detection	High-Z
6	Overtemperature protection	High-Z
7	Output short to supply/GND	Current limit

11. EEPROM Description

11.1 EEPROM List

Page	Row	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	EE_CODE<3>	PWMMS	CAL_LSEL<3:0>				EE_CODE<2>	CalibMASK
	1	PID_FILTER_SEL<1:0>		DP<13:8>					
	2	DP<7:0>							
	3	TRIMBG<2:0>			TRIMOSC<4:0>				
	4	GAIN_TH<1:0>		VOS_TH<1:0>		VOSEN	LC_AMSEL	LC_IREF	G1
	5	EE_CODE<1>	CRCMASK	OTPMASK	OVPMASK	UVLOMASK	RXDMASK	LCFREMASK	LCVPPMASK
	6	ABZEDG<1:0>		ABZ_HYS<1:0>		ABZWID<1:0>		ABZLINE<2:1>	
	7	ABZLINE<0>	PWMCTRL	PWMPOL	PWMT	EE_CODE<0>	DIR	OUTMOD<1:0>	
	8	VOS3_SIN<3:0>				VOS3_COS<3:0>			
	9	G2<3:0>				G3<3:0>			
	A	V3P3EN	G2F_SIN<2:0>			CLK_SLOW	G2F_COS<2:0>		
	B	VOS_SIN_G<7:0>							
	C	VOS_COS_G<7:0>							
	D	VOS_SIN_F<7:0>							
	E	VOS_COS_F<7:0>							
	F	CRC							

11.2 Register Bit Description

Symbol	Bit	R/W	Bit Address	Description
EE_CODE[3:0]	4	R/W	0x00[7]+0x00[1]+0x05[7]+0x07[3]	EEPROM erase/write enabled when EE_CODE = 4'b1100
CalibMASK	1	R/W	0x00[0]	Auto-calibration and auto-zeroing mask: 0 = Enabled; 1 = Disabled
CAL_LSEL[3:0]	4	R/W	0x00[5:2]	Auto-calibration max/min counting duration; 6 = For 60 Hz (calibration done in 10 s)
PID_FILTER_SEL[1:0]	2	R/W	0x01[7:6]	Speed selection: 00 = 600 krpm; 11 = 60 krpm
DP[13:0]	14	R/W	0x01[5:0]+0x02[7:0]	Zero calibration data
GAIN_TH[1:0]	2	R/W	0x04[7]+0x04[6]	On-chip calibration VPP threshold 0x04[7]=0: Coarse adjustment ±15% 0x04[7]=1: Coarse adjustment ±10% 0x04[6]=0: Fine adjustment ≤1.5% 0x04[6]=1: Fine adjustment ≤1%
VOS_TH[1:0]	2	R/W	0x04[5]+0x04[4]	On-chip calibration VOS threshold 0x04[5]=0: Coarse adjustment ±2‰ 0x04[5]=1: Coarse adjustment ±1‰ 0x04[4]=0: Fine adjustment ≤2‰ 0x04[4]=1: Fine adjustment ≤1‰
VOSEN	1	R/W	0x04[3]	Internal VOS enable: 0 = VOS disabled; 1 = VOS enabled
LC_AMSEL	1	R/W	0x04[2]	LC output VPP selection: 0 = 2.8 V; 1 = 3.8 V
G1	1	R/W	0x04[0]	1st-stage gain selection: 0 = ×2; 1 = ×4
CRCMASK	1	R/W	0x05[6]	CRC diagnostic mask: 0 = Enabled; 1 = Disabled
OTPMASK	1	R/W	0x05[5]	OTP diagnostic mask: 0 = Enabled; 1 = Disabled
OVPMASK	1	R/W	0x05[4]	OVP diagnostic mask: 0 = Enabled; 1 = Disabled
UVLOMASK	1	R/W	0x05[3]	UVLO diagnostic mask: 0 = Enabled; 1 = Disabled
RXDMASK	1	R/W	0x05[2]	RX_OPEN diagnostic mask: 0 = Enabled; 1 = Disabled
LCFREMASK	1	R/W	0x05[1]	LC frequency diagnostic mask: 0 = Enabled; 1 = Disabled
LCVPPMASK	1	R/W	0x05[0]	LC amplitude diagnostic mask: 0 = Enabled; 1 = Disabled
ABZEDG[1:0]	2	R/W	0x06[7:6]	Edge alignment between Z pulse and AB pulses: 0: Z rising edge aligns with B rising edge 1: Z rising edge aligns with B falling edge 2: Z rising edge aligns with A falling edge 3: Z rising edge aligns with A rising edge
ABZHYS	2	R/W	0x06[5:4]	Hysteresis setting for ABZ signals: 0: 0.25×T; 1: 0.5×T; 2: 0.75×T; 3: 1×T
ABZWID	2	R/W	0x06[3:2]	Z pulse width setting in ABZ signals: 0: 0.25×T; 1: 0.5×T; 2: 1×T; 3: 180°
ABZLINE	3	R/W	0x06[2:0]+0x07[7]	Line count per revolution for ABZ: 0: 12 lines; 1: 24 lines; 2: 50 lines; 3: 128 lines; 4: 256 lines; 5: 512 lines; 6: 1024 lines; 7: 2048 lines

EEPROM Explanation of Table Sequence

Symbol	Bit	R/W	Bit Address	Description
PWMCTRL	1	R/W	0x07[6]	0 : PWM flag output; 1 : Normal PWM output
PWMPOL	1	R/W	0x07[5]	0 : PWM active low; 1 : PWM active high
PWMT	1	R/W	0x07[4]	PWM output frequency: 0 : 250 Hz; 1 : 1000 Hz
DIR	1	R/W	0x07[2]	Rotation direction configuration:0: CW : A leads B; CCW : B leads A1: CW : B leads A; CCW : A leads B
OUTMOD[1:0]	2	R/W	0x07[1:0]	Output mode configuration:0 : SPI mode; 1 : ABZ+PWM mode; 2 : Analog sine/cosine output mode; 3 : SPI mode
VOS3_SIN[3:0]	4	R/W	0x08[7:4]	3rd-stage VOS compensation for SIN channel
VOS3_COS[3:0]	4	R/W	0x08[3:0]	3rd-stage VOS compensation for COS channel
G2[3:0]	4	R/W	0x09[7:4]	2nd-stage gain adjustment: 8~123 ×1.2
G3[3:0]	4	R/W	0x09[3:0]	3rd-stage gain adjustment: 1~4 ×1.1
V3P3EN	1	R/W	0x0A[7]	3.3 V application flag
G2F_SIN[2:0]	3	R/W	0x0A[6:4]	Fine gain adjustment for SIN channel
CLK_SLOW	1	R/W	0x0A[3]	ADC sampling clock: 0 : 8 MHz; 1 : 16 MHz
G2F_COS[2:0]	3	R/W	0x0A[2:0]	Fine gain adjustment for COS channel
VOS_SIN_G[7:0]	8	R/W	0x0B[7:0]	Coarse VOS compensation for SIN channel
VOS_COS_G[7:0]	8	R/W	0x0C[7:0]	Coarse VOS compensation for COS channel
VOS_SIN_F[7:0]	8	R/W	0x0D[7:0]	Fine VOS compensation for SIN channel
VOS_COS_F[7:0]	8	R/W	0x0E[7:0]	Fine VOS compensation for COS channel
CRC	8	R	0x0F[7:0]	CRC checksum

12. ABZ/PWM output

Typical application diagram

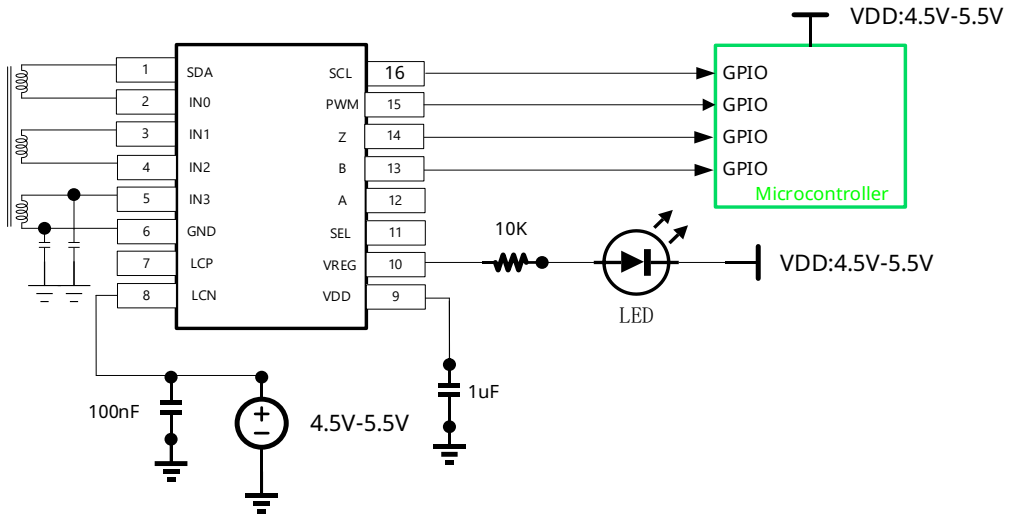


Fig.5 Incremental output application diagram

ABZ output waveform diagram

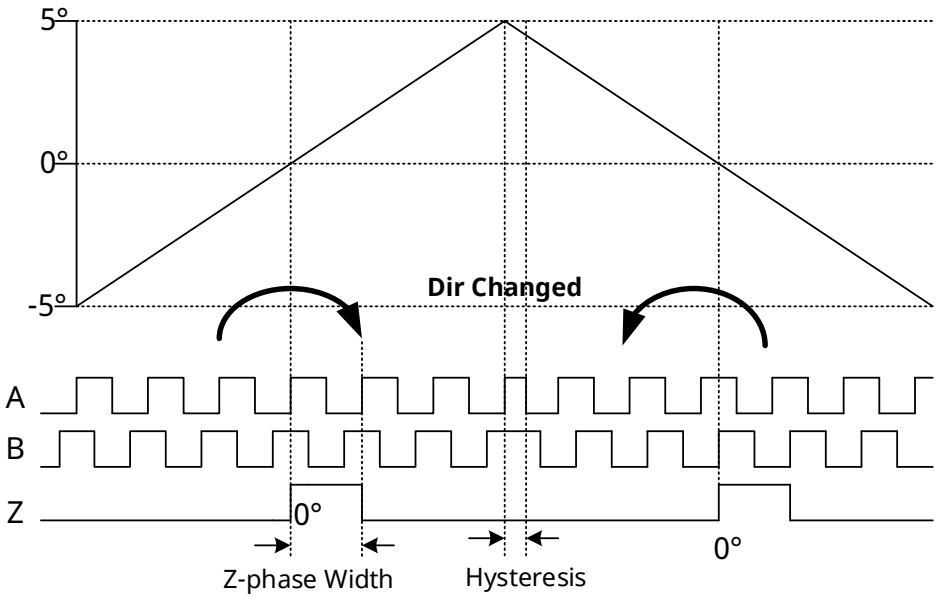


Fig.6 Incremental output waveform diagram

PWM output waveform diagram

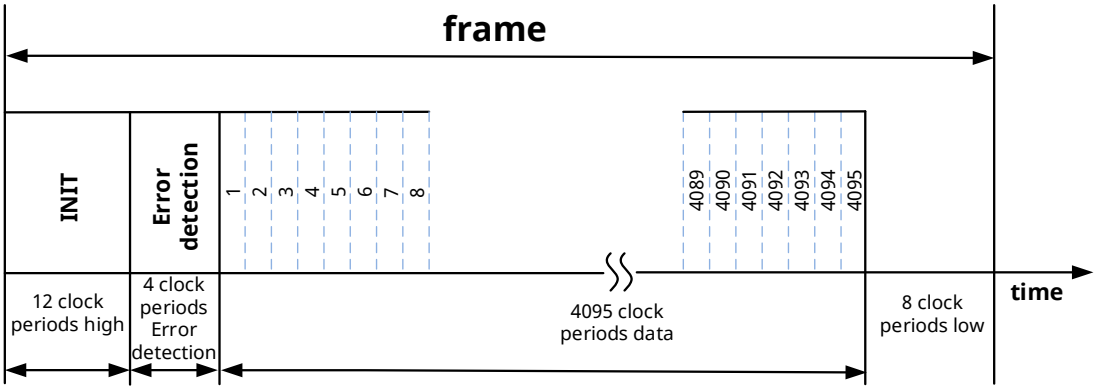


Fig.7 Clamped PWM output waveform diagram

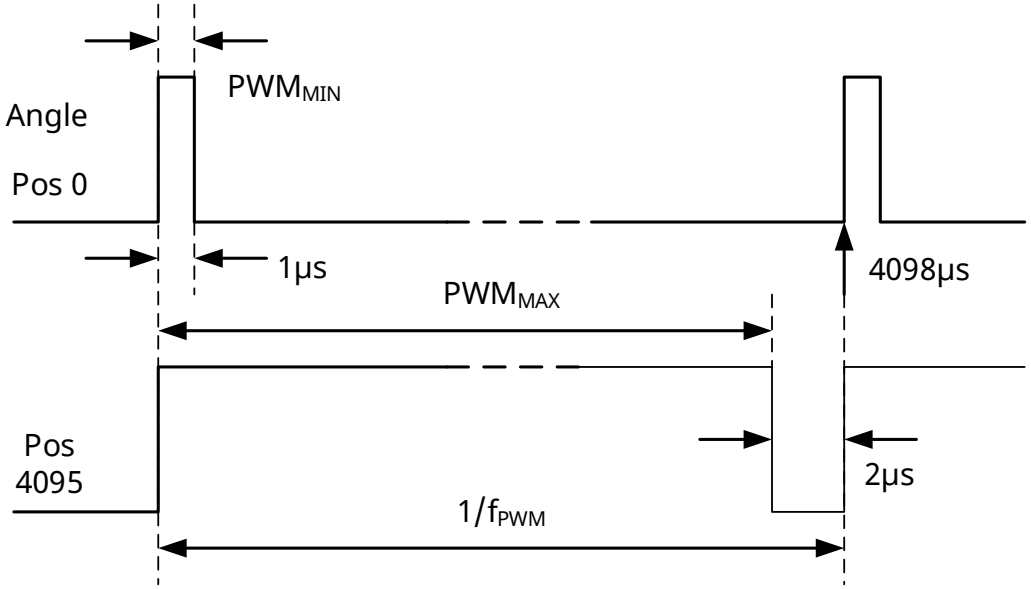


Fig.8 Normal PWM output waveform diagram

13. SPI Output

SPI timing diagram

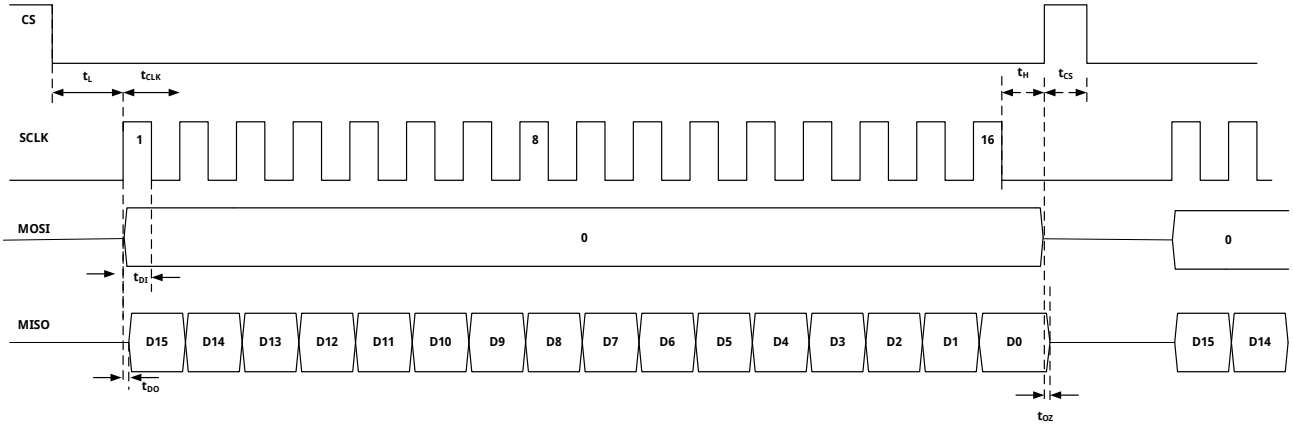


Fig.9 SPI Angle Output Diagram

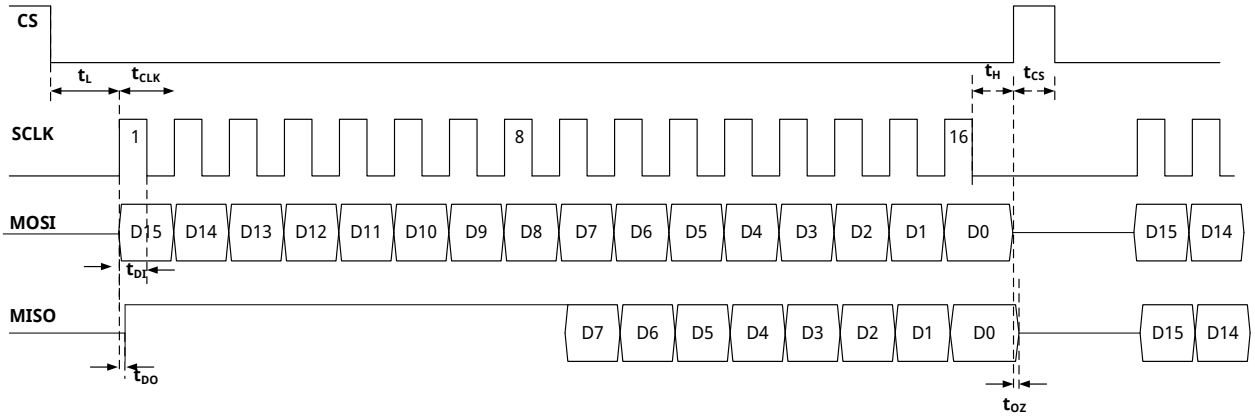


Fig.10 3.3V Communication timing diagram

Description of the 16-bit MOSI data frame for SPI

In angle output mode, send 16'hFF01 to enter the normal SPI communication mode

Bit	Name	Description
D15-D12	CMD	Command frame
D11-D8	ADDR	Address frame
D7-D0	DF1	Data frame

Description of SPI Command CMD

Name	Code	Description
EE_BYTE_WR	4'b0001	Write received DATA to the corresponding EEPROM address
EE_BLOCK_WR	4'b0010	Write all values from EEPROM mirror registers to EEPROM
EE_BTYE_RD	4'b0011	Read EEPROM data from the corresponding address
EE_LOAD	4'b0100	Load all EEPROM data into mirror registers
REG_SH_RD	4'b0101	Read shadow registers
REG_SH_WR	4'b0110	Write shadow registers
REG_NR_RD	4'b0111	Read internal function registers
REG_NR_WR	4'b1000	Write internal function registers
EE_SLEEP	4'b1001	Disable EEPROM
EE_WAKE	4'b1010	Enable EEPROM
EE_MBIST	4'b1110	Execute MBIST

14. Power Supply Connection Configuration

5V Application Circuit Connection

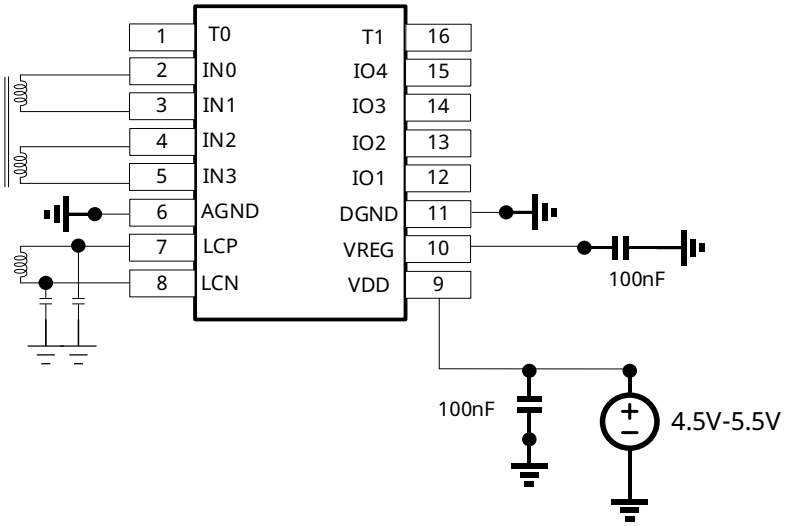


Fig.11 5V Power supply circuit diagram

3.3V Application Circuit Connection

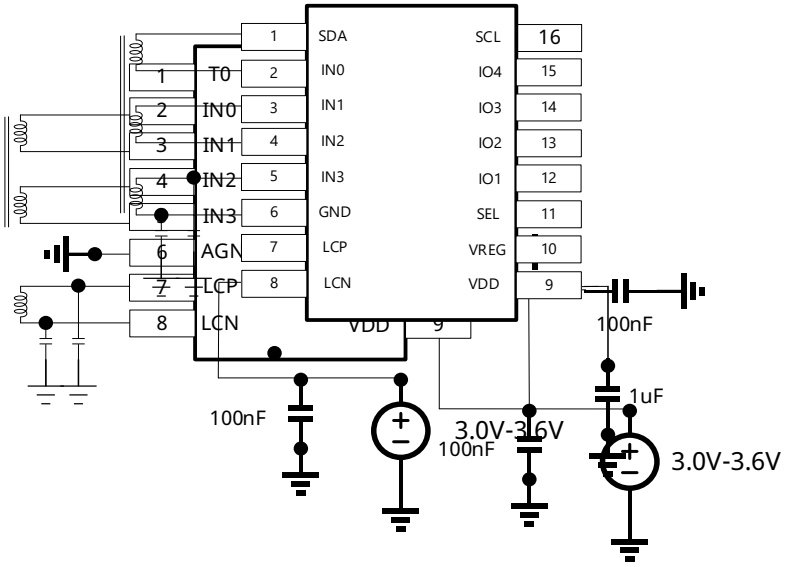


Fig.12 3.3V Power supply circuit diagram

15. Self-calibration and zero-adjustment peripheral circuits

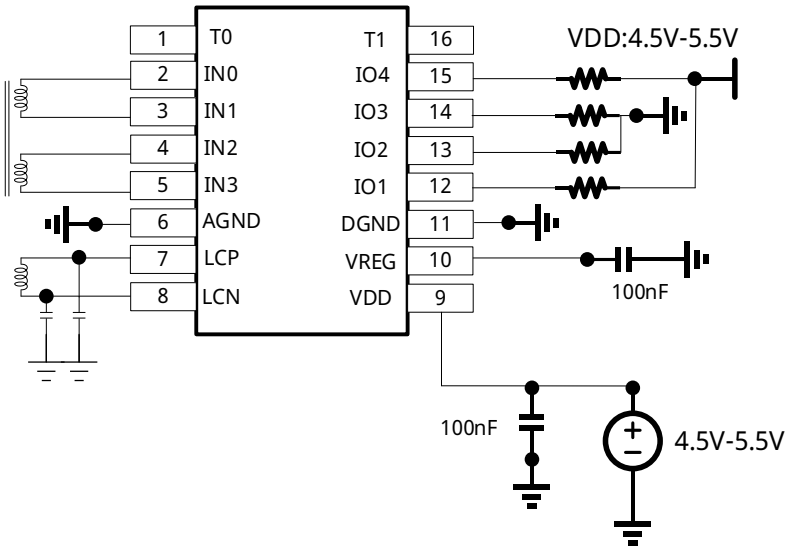


Fig.13 Peripheral circuit for self-calibration mode

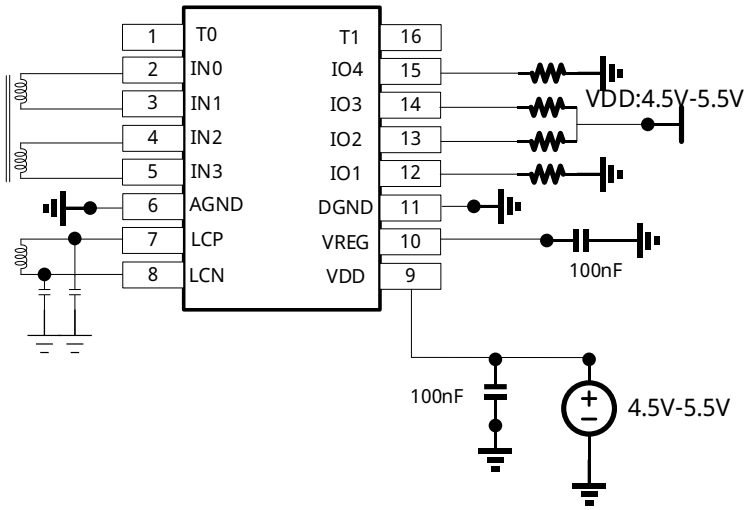


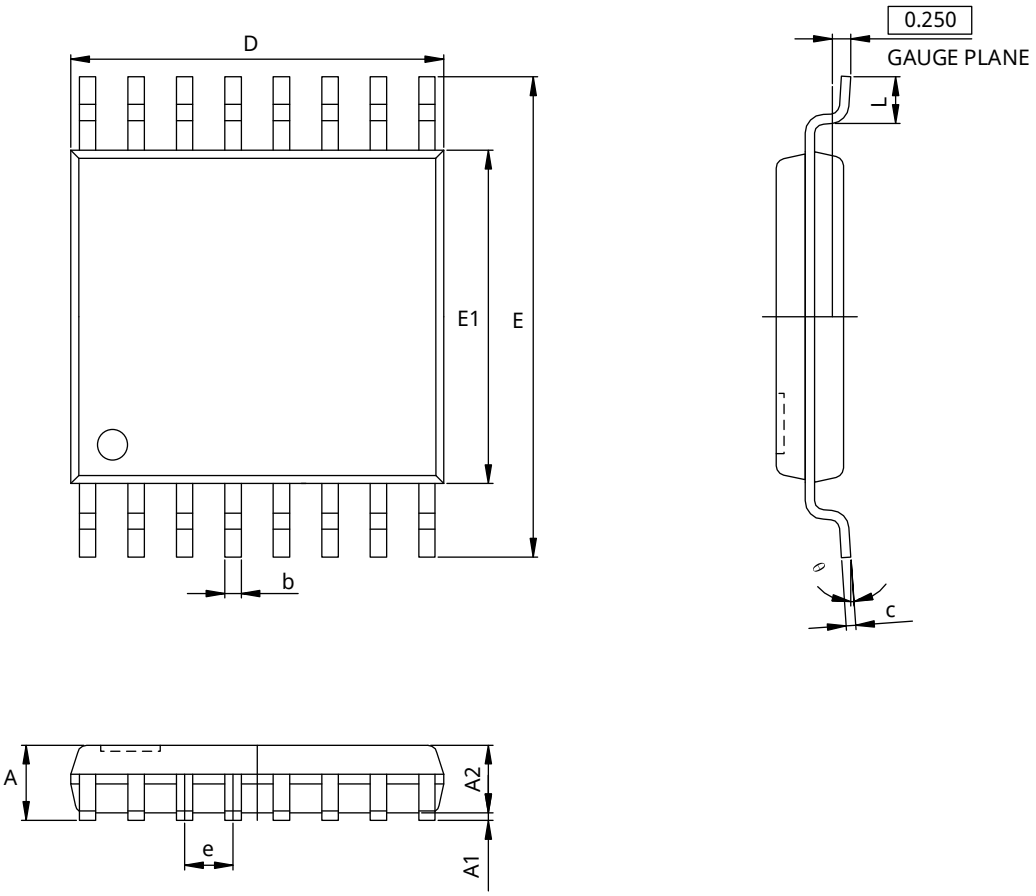
Fig.14 Peripheral circuit for zero adjustment mode

Note:

Resistors on IO0–IO4 are only used to trigger auto-calibration and zero-setting. This function can be implemented externally using a small adapter board. These resistors must be removed in actual application, and the peripheral circuit shall be built according to the application schematic.

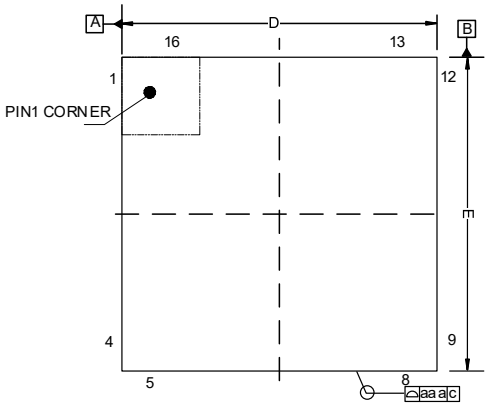
16. Package Information

16.1. TSSOP16 Package (TG)

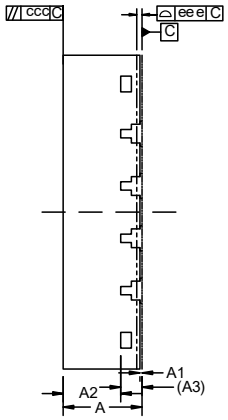


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.252(BSC)	
E1	4.300	4.500	0.169	0.177
e	0.650(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

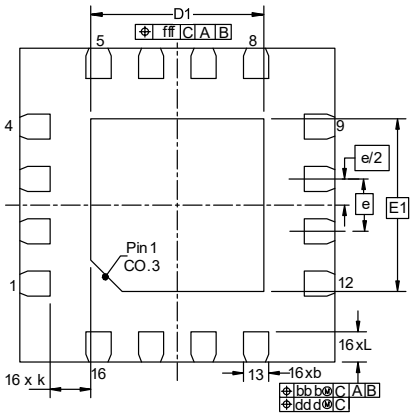
16.2. QFN3*3-16 Package (QC)



TOP VIEW



SIDE VIEW



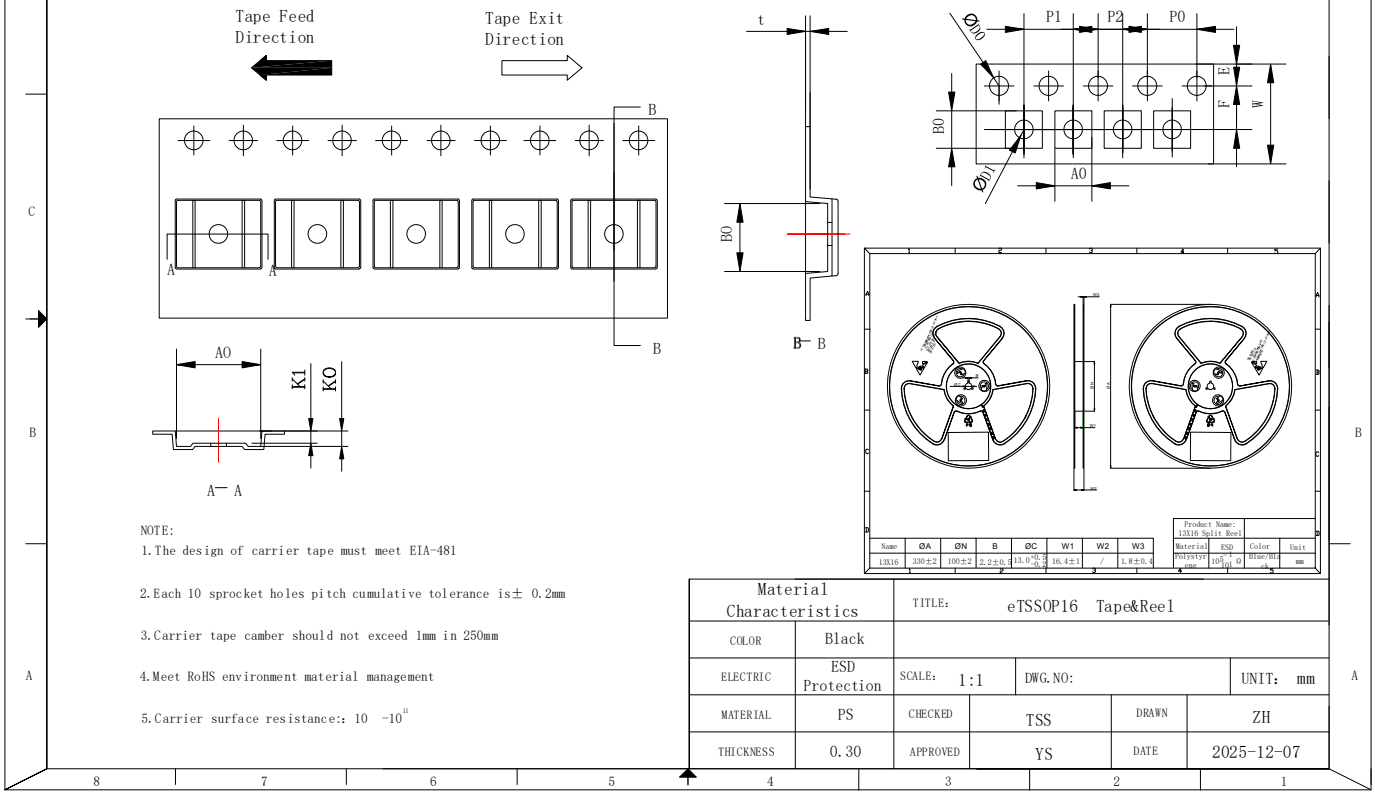
BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0.00	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
BODY SIZE	X	D	3.00 BSC		
	Y	E	3.00 BSC		
EP SIZE	X	D1	1.50	1.65	1.80
	Y	E1	1.50	1.65	1.80
LEAD WIDTH		b	0.18	0.24	0.30
LEAD PITCH		e	0.500 BSC		
LEAD TIP TO EXPOSED PAD EDGE		k	0.385 BSC		
LEAD LENGTH		L	0.19	0.29	0.39
PACKAGE EDGE TOLERANCE		aaa	0.1000		
MOLD FLATNESS		ccc	0.1000		
COPLANARITY		eee	0.0800		
LEAD OFFSET		bbb	0.1000		
		ddd	0.0500		
EXPOSED PAD OFFSET		fff	0.1000		

17. Package Specification

17.1. TSSOP16 Package (TG)

Specifications	W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	K0	K1	t
Size	16.00 ±0.30	1.75 ±0.10	7.50 ±0.10	1.50 +0.10	1.50 +0.10	4.00 ±0.10	2.00 ±0.10	40.00 ±0.20	8.00 ±0.10	6.80 ±0.10		5.40 ±0.10		1.60 ±0.10	1.30 ±0.10	0.30 ±0.05

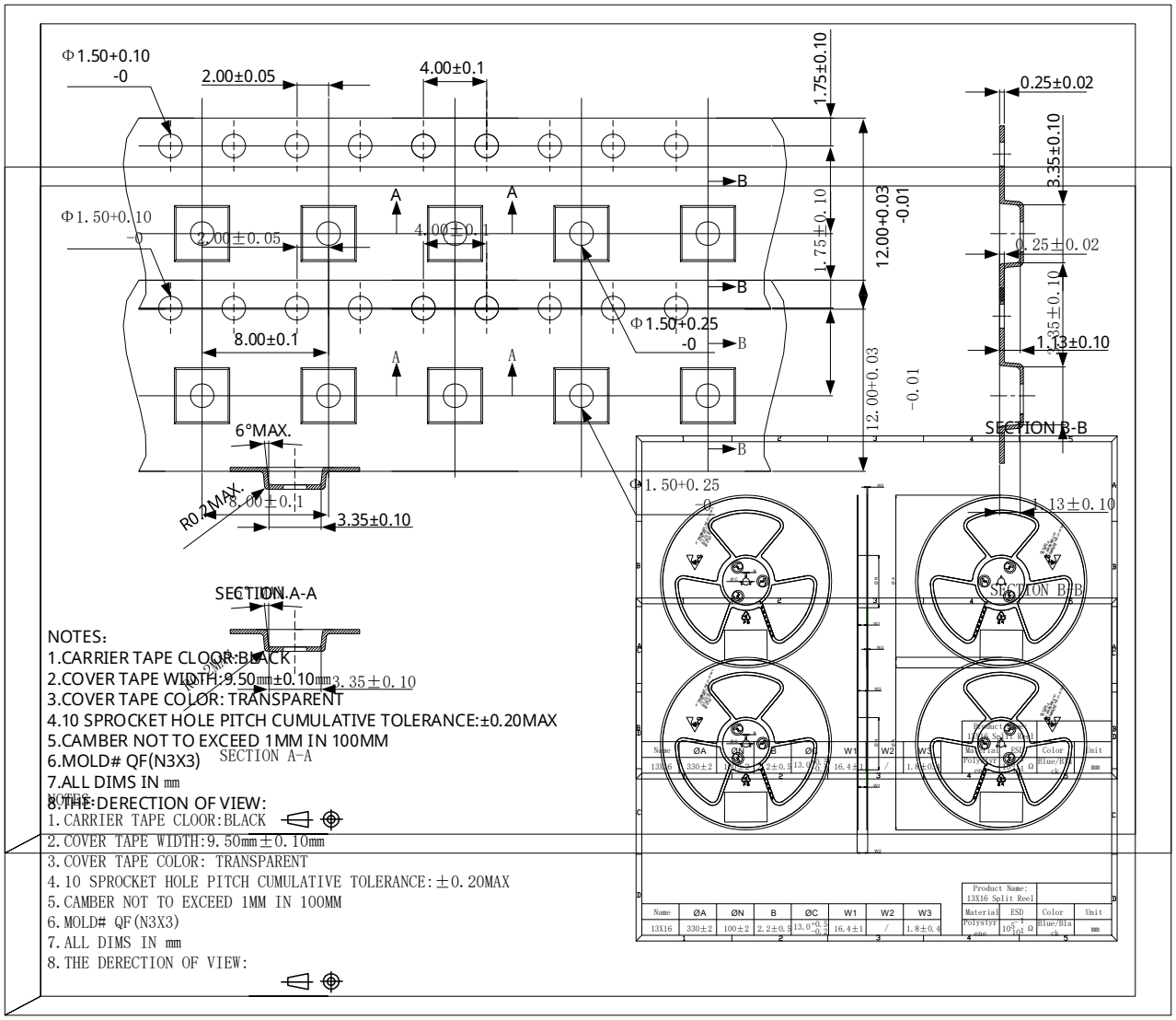


NOTE:

1. The design of carrier tape must meet EIA-481
2. Each 10 sprocket holes pitch cumulative tolerance is± 0.2mm
3. Carrier tape camber should not exceed 1mm in 250mm
4. Meet RoHS environment material management
5. Carrier surface resistance:: 10 ^{4} -10 ^{11}

Material Characteristics		TITLE:	eTSSOP16 Tape&Reel		
COLOR	Black				
ELECTRIC	ESD Protection	SCALE: 1:1	DWG.NO:		UNIT: mm
MATERIAL	PS	CHECKED	TSS	DRAWN	ZH
THICKNESS	0.30	APPROVED	YS	DATE	2025-12-07

17.2. QFN3*3-16 Package (QC)



18. Revision History

Revision	Date	Description
Rev.V0.1	2025-12-10	Preliminary datasheet
Rev.V0.2	2026-01-11	Add the packing information, Update output-pin define

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