60V 4-Switch Buck-Boost Controller

DESCRIPTION

The VE8620 is a synchronous 4-switch buck-boost voltage/current regulator controller. The VE8620 can regulate output voltage, output current, or input current with input voltages above, below, or equal to the output voltage.

The VE8620 uses the proprietary buck-boost control algorithm with peak current mode for boost and valley current mode for buck.

The constant-frequency, current mode architecture allows its frequency to be adjusted from 100KHz to 700KHz. No top FET refresh switching cycle is needed in buck or boost operation. With 60V input, 60V output capability and seamless transitions between operating regions, the VE8620 is ideal for voltage regulator, battery/super-capacitor charger applications in automotive, industrial, telecom, and even battery-powered systems.

The VE8620 provides input current monitor, output current monitor, and various status flags, such as C/10 charge termination and shorted output flag.
The VE8620 is available in TSSOP38-EP package. This package use EPAD to improve thermal performance and noise immunity.

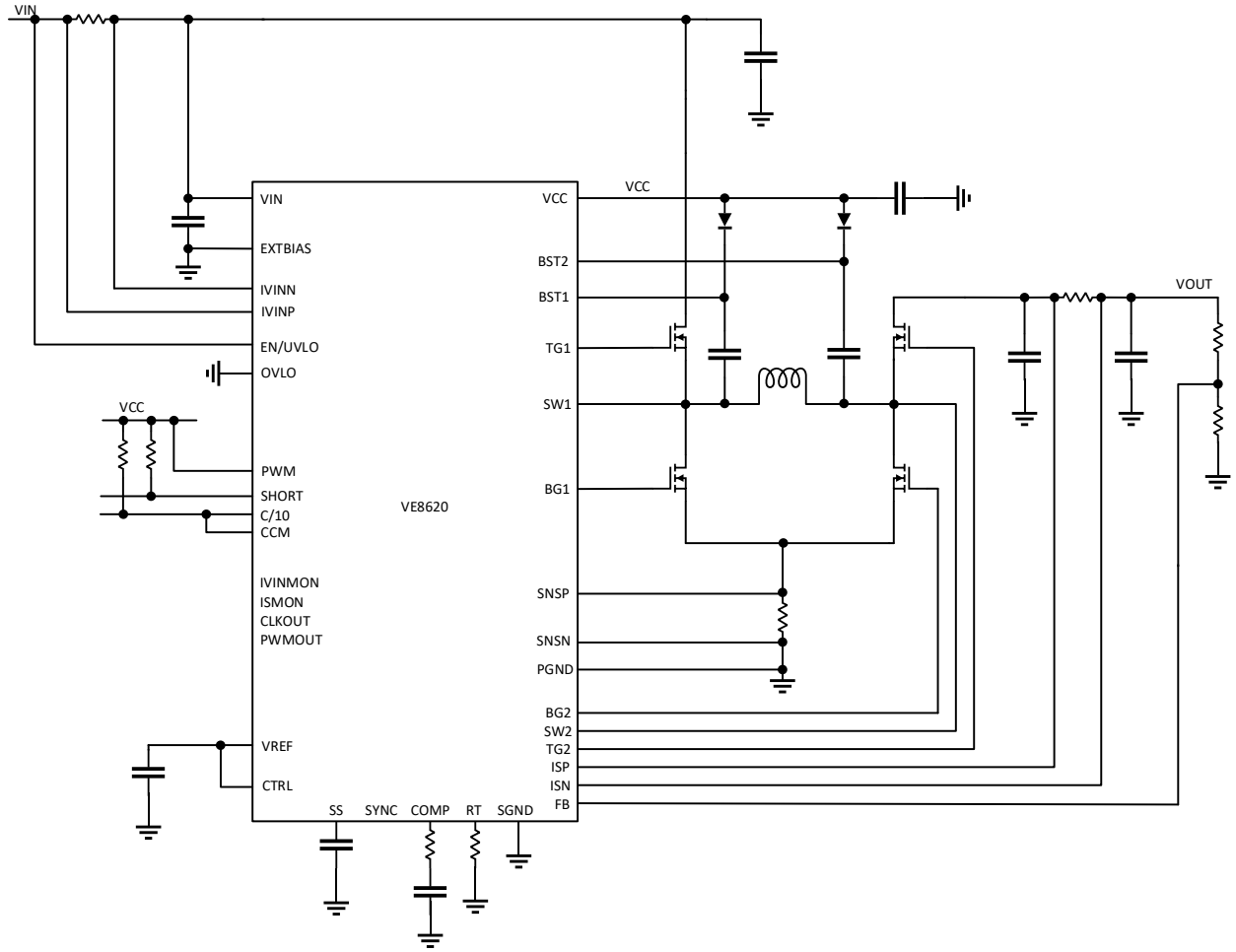
FEATURES

- 4-Switch Single Inductor Architecture Allows VIN Above, Below or Equal to VOUT
- Synchronous Switching: Up to 98.5% Efficiency
- Wide VIN Range: 4.5V to 60V
- 1.5% Output Voltage Accuracy:
  1.2V ≤ VOUT ≤ 60V
- 6% Output Current Accuracy:
  3V ≤ VOUT ≤ 60V
- Input and Output Current Regulation with Current Monitor Outputs
- No Top FET Refresh in Buck or Boost
- VOUT Disconnected from VIN During Shutdown
- C/10 Charge Termination and Output Shorted Flags
- Easy Parallel Capability to Extend Output Power
- 38-Lead TSSOP with Exposed Pad

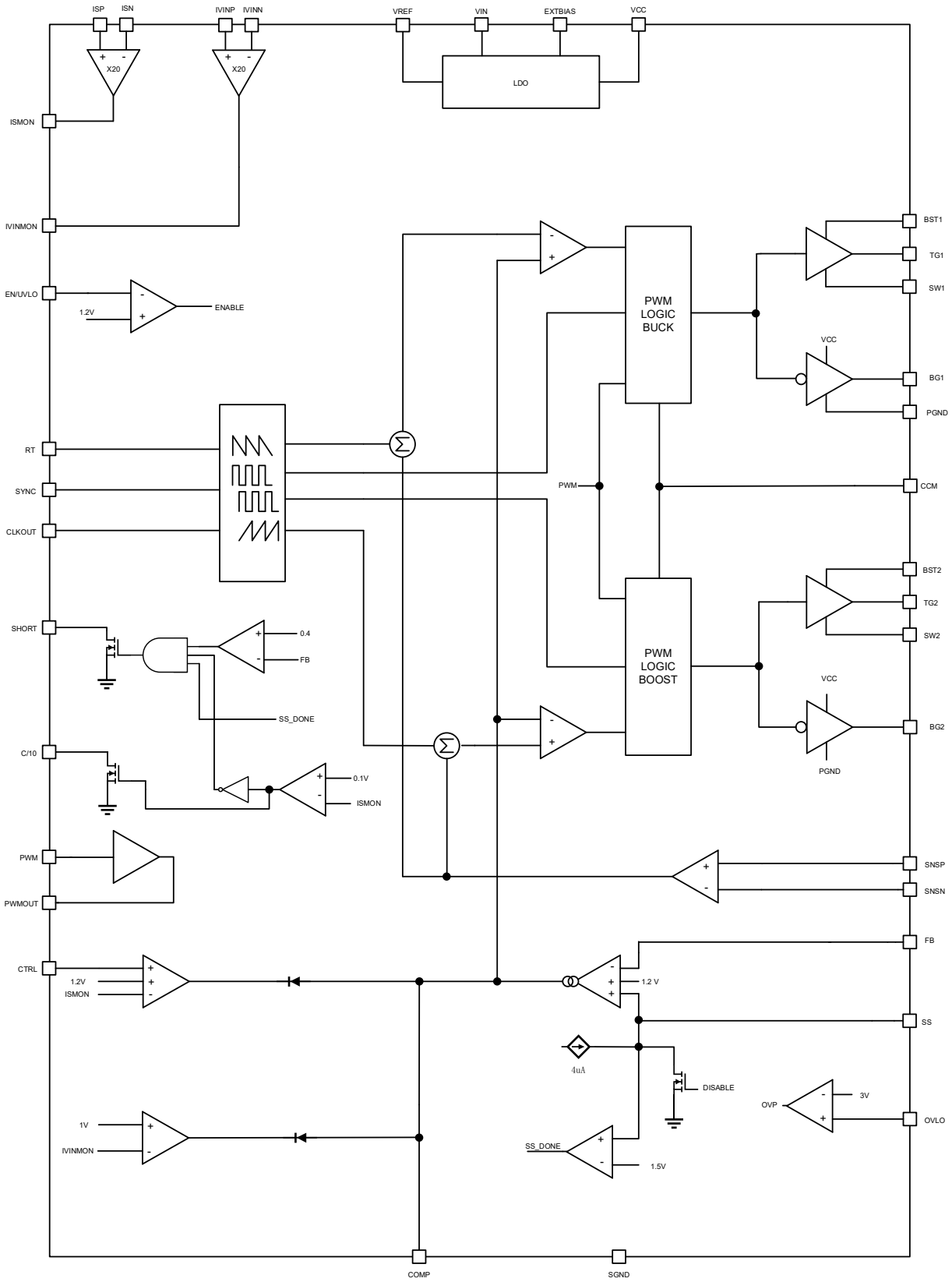
APPLICATIONS

- Automotive, Telecom, Industrial Systems
- High Power Battery-Powered System

TYPICAL APPLICATION



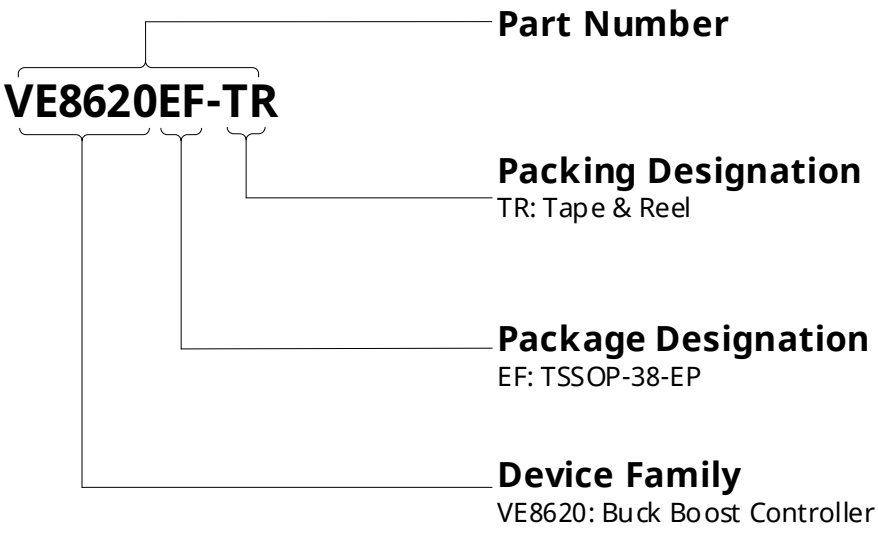
BLOCK DIAGRAM



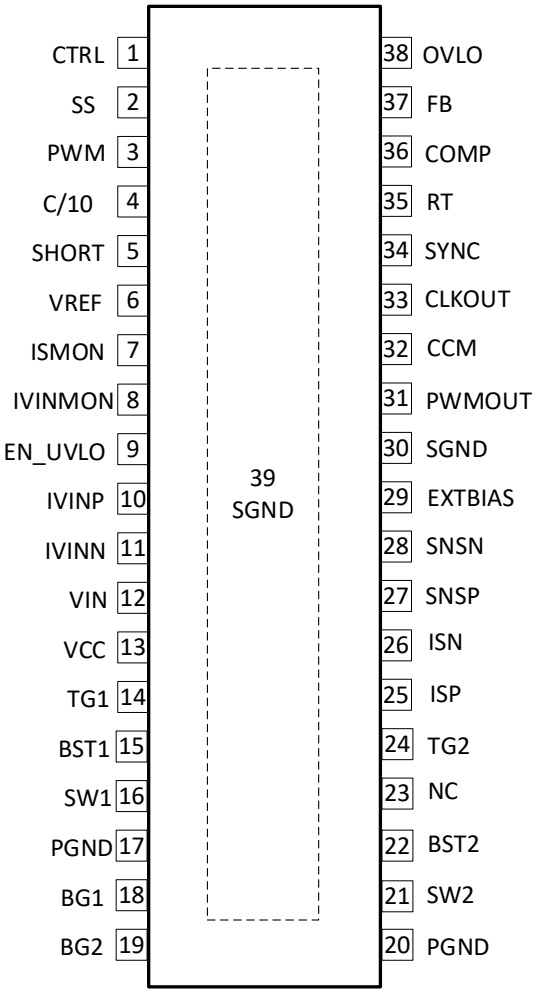
ORDERING INFORMATION

Ordering Information	Mark	Temperature Range	Package	Pack	Quantity
VE8620EF-TR	8620	-40 to +125°C	TSSOP-38-EP	TR	4000
VE8620P(1)		-40 to +125°C			

Note 1: This product is available only in wafer form and is not offered in packaged versions.



PIN CONFIGURATIONS



PIN DESCRIPTION

Pin	Name	Description
1	CTRL	Output Current Sense Threshold Adjustment Pin. Regulating threshold $V_{(ISP-ISN)}$ is 1/20th of V_{CTRL}. CTRL linear range is from 0V to 1.1V. For V_{CTRL} > 1.4V, the current sense threshold is constant at the full-scale value of 60mV. Connect CTRL to VREF for the 60mV default threshold. Force less than 50mV (typical) to stop switching. Do not leave this pin open.
2	SS	A regulated 4uA current charges up the SS capacitor. The value of this SS capacitor sets the output voltage ramp.
3	PWM	A signal low turns off switches, idles switching and disconnects the COMP pin from all external loads. The PWMOUT pin follows the PWM pin. If not used, connect to VCC.
4	C/10	C/10 Charge Termination Pin. An open-drain pull-down on C/10 asserts if V_{ISMON} is less than 100mV (typical). To function, the pin requires an external pull-up resistor.

Pin	Name	Description
5	SHORT	Output Shorted Pin. An open-drain pull-down on SHORT asserts if FB is less than 400mV (typical) and V_{ISMON} is larger than 120mV (typical). To function, the pin requires an external pull-up resistor.
6	VREF	Voltage Reference Output Pin, typically 2V. Can supply up to 2mA of current.
7	ISMON	Monitor pin that produces a voltage that is twenty times the voltage $V_{(ISP-ISN)}$. ISMON will equal 1.2V when $V_{(ISP-ISN)}$ = 60mV. For parallel applications, tie master VE8620 ISMON pin to slave VE8620 CTRL pin.
8	IVINMON	Monitor pin that produces a voltage that is twenty times the voltage $V_{(IVINP-IVINN)}$. IVINMON will equal 1V when $V_{(IVINP-IVINN)}$ = 50mV.
9	EN/UVLO	Enable Control Pin. Forcing an accurate 1.2V falling threshold with 120mV hysteresis. An undervoltage condition resets soft-start. Tie to 0.3V, or less, to disable the device.
10	IVINP	Positive Input for the Input Current Limit and Monitor. Input bias current for this pin is typically 300μA.
11	IVINN	Negative Input for the Input Current Limit and Monitor.
12	VIN	Main Input Supply. Bypass this pin to PGND with a capacitor.
13	VCC	Internal 5V Regulator Output. The driver and control circuits are powered from this voltage. Bypass this pin to PGND with a minimum 4.7μF ceramic capacitor.
14	TG1	Top Gate Drive. Drives the top N-channel MOSFET.
15	BST1	Bootstrapped Driver Supply. Connect a bypass capacitor between BST1 and SW1.A Schottky or high-speed diode must be tied from VCC to BST1.
16	SW1	Switch Node.
17/20	PGND	Power Ground.
18	BG1	Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and VCC.
19	BG2	Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and VCC.
21	SW2	Switch Node.
22	BST2	Bootstrapped Driver Supply. Connect a bypass capacitor between BST2 and SW2.A Schottky or high-speed diode must be tied from VCC to BST2.
23	NC	No Connect Pin. Leave this pin floating.
24	TG2	Top Gate Drive. Drives the top N-channel MOSFET.
25	ISP	Connection Point for the Positive Terminal of the Output Current Feedback Resistor. Input bias current for this pin is typically 300μA.
26	ISN	Connection Point for the Negative Terminal of the Output Current Feedback Resistor.
27	SNSP	The Positive Input to the Current Sense Comparator.
28	SNSN	The Negative Input to the Current Sense Comparator.
29	EXTBIAS	External bias input for the optional VCC LDO. There is an internal switch to disconnect the VIN LDO when EXTBIAS voltage is higher than 4.7V. Decouple this pin to ground with a ≥1μF ceramic capacitor when it is in use. Connect this pin to ground if it is not used.
30	SGND	Signal Ground. All small-signal components and compensation should connect

Pin	Name	Description
		to this ground, which should be connected to PGND at a single point. Solder the exposed pad directly to the ground plane.
31	PWMOUT	Buffered Version of PWM Signal for Driving Output Load Disconnect N-Channel MOSFET. The PWMOUT pin is driven from VCC. Use of a MOSFET with a gate cutoff voltage higher than 1V is recommended.
32	CCM	Continuous Conduction Mode Pin. When the pin voltage is higher than 1.5V, the part runs in fixed frequency forced continuous conduction mode and allows the inductor current to flow negative. When the pin voltage is less than 0.3V, the part runs in discontinuous conduction mode and does not allow the inductor current to flow backward. This pin is only meant to block inductor reverse current, and should only be pulled low when the output current is low. This pin must be either connected to VCC for continuous conduction mode across all loads, or it must be connected to the C/10 with a pull-up resistor to VCC for continuous conduction mode at heavy load and for discontinuous conduction mode at light load.
33	CLKOUT	Clock Output Pin. A 180° out-of-phase clock is provided at the oscillator frequency to allow for paralleling two devices for extending output power capability.
34	SYNC	External Synchronization Input Pin. The internal buck clock is synchronized to the rising edge of the SYNC signal while the internal boost clock is 180° phase shifted.
35	RT	Frequency Set Pin. Place a resistor to GND to set the internal frequency. The range of oscillation is 100kHz to 700kHz.
36	COMP	Regulation control loop compensation. Connect an R-C network from COMP to SGND to compensate for the regulation control loop.
37	FB	Voltage Loop Feedback Pin. FB is intended for constant-voltage regulation. The internal transconductance amplifier with output COMP will regulate FB to 1.2V through the DC/DC converter.
38	OVLO	Overvoltage Input Pin. This pin is used for OVLO, if OVLO > 3V then SS is pulled low, the part stops switching and resets. Do not leave this pin open. Connect this pin to ground if it is not used.
39	Exposed Pad	Signal Ground. Solder the exposed pad directly to the ground plane.

ABSOLUTE MAXIMUM RATINGS

Parameter	Minimum	Maximum	Unit
VIN	-0.3	+65	V
EXTBIAS	-0.3	+26	
SW1, SW2	-0.3(-5V 20ns)	+65	V
C/10, SHORT	-0.3	+15	V
EN/UVLO, IVINP, IVINN, ISP, ISN	-0.3	+65	V
VCC, BST1-SW1, BST2-SW2	-0.3	+6.5	V
IVINP-IVINN, ISP-ISN,SNSP-SNSN	-0.3	+0.3	V
SNSP, SNSN	-0.3	+0.3	V
Other Pins	-0.3	+6.5	V
Storage Temperature	-65	+150	°C

RECOMMENDED OPERATINIG CONDITIONS

Parameter	Minimum	Maximum	Unit
VIN	+4.5	+60	V
EXTBIAS	+4.7	+24	V
VOUT	+1.2	+60	V
Operating Junction Temperature	-40	+125	°C

THERMAL INFORMATION

Thermal Resistance	θ_{JA}(°C/W)	θ_{JC}(°C/W)
TSSOP38	28	2

ECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted.

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Input							
V_{IN} Operating Voltage	V_{IN}		●	4.5		60	V
V_{IN} Shutdown I_Q	I_{shut}	$V_{EN/UVLO}$ = 0V			2		μA
V_{IN} Operating I_Q (Not Switching)	I_Q	FB = 1.3V, RT = 90k			3.0		mA
Logic Inputs							
EN/UVLO Rising Threshold	V_{EN}		●		1.2		V
EN/UVLO Hysteresis			●		120		mV
EN/UVLO Pin Bias Current High		$V_{EN/UVLO}$ = 2V			1		uA
CCM Threshold Voltage				0.3		1.5	V
CTRL Latch-Off Threshold		Rising			50		mV
CTRL Latch-Off Hysteresis					13		mV
OVLO Rising Shutdown Voltage		VCC = 5V	●		3		V
OVLO Falling Hysteresis		VCC = 5V			90		mV
Regulation							
VREF Voltage			●		2		V
$V_{(ISP-ISN)}$ Threshold		V_{CTRL} = 2V, V_{ISP} = 12V	●		60		mV
		V_{CTRL} = 2V, V_{ISP} = 1V			60		mV
		V_{CTRL} = 1V, V_{ISP} = 12V	●		50		mV
		V_{CTRL} = 1V, V_{ISP} = 1V			50		mV
		V_{CTRL} = 0.6V, V_{ISP} = 12V	●		30		mV
		V_{CTRL} = 0.6V, V_{ISP} = 1V			30		mV
		V_{CTRL} = 0.1V, V_{ISP} = 12V	●		5		mV
		V_{CTRL} = 0.1V, V_{ISP} = 1V			5		mV
ISP Bias Current		V_{ISP} = 12V, V_{ISN} = 12V			270		μA
ISN Bias Current		V_{ISP} = 12V, V_{ISN} = 12V				1	μA
Output Current Sense Common Mode Range				0		60	V

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Current Sense Amplifier gm					250		μS
ISMON Monitor Voltage		V_{ISP}=12V $V_{(ISP-ISN)}$ = 60mV	●		1.2		V
		V_{ISP}=12V $V_{(ISP-ISN)}$ = 0V	●			50	mV
$V_{(IVINP-IVINN)}$ Threshold		V_{IVINP}=12V	●		50		mV
IVINP Bias Current		V_{IVINP} = V_{IVINN} = 12V			270		μA
IVINN Bias Current		V_{IVINP} = V_{IVINN} = 12V				1	μA
Input Current Sense Common Mode Range				0		60	V
Input Current Sense Amplifier gm					250		uS
IVINMON Monitor Voltage		V_{IVINP}=12V $V_{(IVINP-IVINN)}$ = 50mV	●		1		V
		V_{IVINP}=12V $V_{(IVINP-IVINN)}$ = 0V	●		30		mV
FB Regulation Voltage		VIN=12V	●		1.2		V
FB Amplifier gm					500		μS
FB Pin Input Bias Current		FB in Regulation				100n	nA
VSENSE(MAX) (VSNSP-SNSN)		Boost	●	46	55	60	mV
		Buck	●	-50	-40	-30	mV
Fault							
SS Pull-Up Current		VSS = 0V			4		μA
C/10 Falling Threshold (V_{ISMON})		VFB = 1.2V			100		mV
SHORT Falling Threshold (V_{FB})					400		mV
C/10 Pin Output Impedance					0.2		kΩ
SHORT Pin Output Impedance					0.2		kΩ
SS Reset Threshold					0.2		V
Oscillator							
Switching Frequency		RT =90k			500		kHz

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
		MAX		700			kHz
		MIN				100	kHz
SYNC Frequency				150		400	kHz
SYNC Pin Resistance to GND					200		kΩ
SYNC Threshold Voltage				0.3		1.5	V
V_{CC} Regulator							
V_{CC} Regulation Voltage		I_{VCC}=0A	●		5		V
		I_{VCC}=10mA	●		4.99		V
V_{CC} Undervoltage Lockout					3.5		V
V_{CC} Current Limit		V_{CC} = 4V			67		mA
VCC from EXTBIAS Regulation Voltage					5		V
EXTBIAS UVLO threshold (rising)					4.68		V
EXTBIAS UVLO threshold (falling)					4.42		V
EXTBIAS current Limit					110		mA
PWM							
PWM Threshold Voltage				0.3		1.5	V
PWM Pin Resistance to GND					200		kΩ
PWMOUT Pull-Up Resistance					30		Ω
PWMOUT Pull-Down Resistance					25		Ω
Driver							
TG1, TG2 Gate Driver On-Resistance		Gate Pull-Up, $V_{BST} – V_{SW}$ = 5V			2		Ω
		Gate Pull-Down , $V_{BST} – V_{SW}$ = 5V			1		Ω
BG1, BG2 Gate Driver On-Resistance		Gate Pull-Up, $V_{BST} – V_{SW}$ = 5V			2		

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
		Gate Pull-Down, $V_{BST} - V_{SW}$ = 5V			1		Ω
TG1, TG2, tOFF(MIN)		RT = 90k			200		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 35V, V_{OUT} = 24V, F_{sw} = 300 kHz, T_J = -40°C to +125°C, unless otherwise noted.

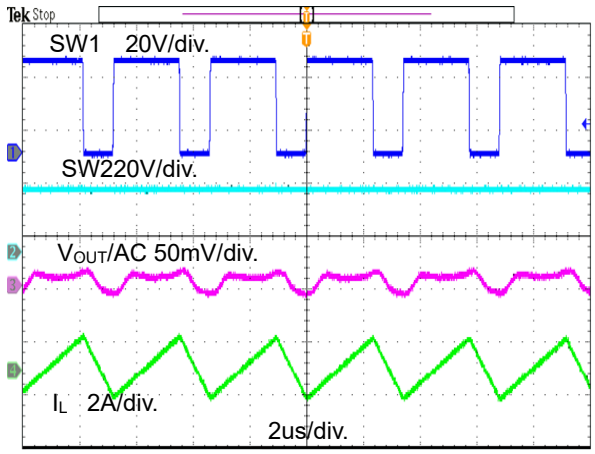


Figure 1. Steady State I_{OUT}=0A CCM

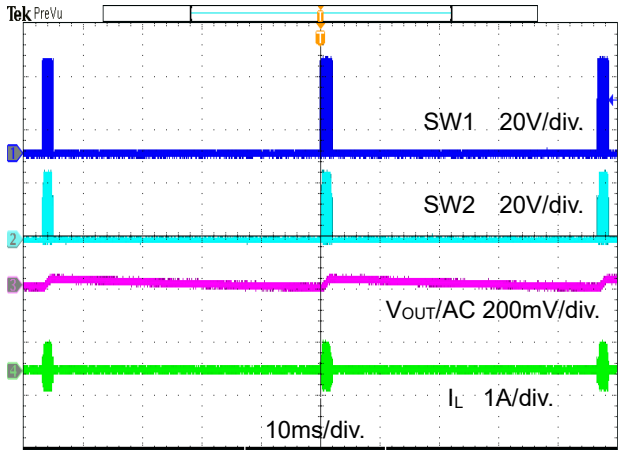


Figure 2. Steady State I_{OUT}=0A DEM

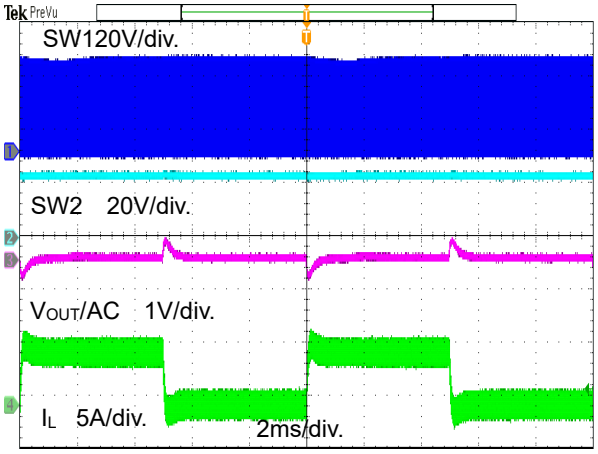


Figure 3. Dynamic Load I_{OUT}=0-5A CCM

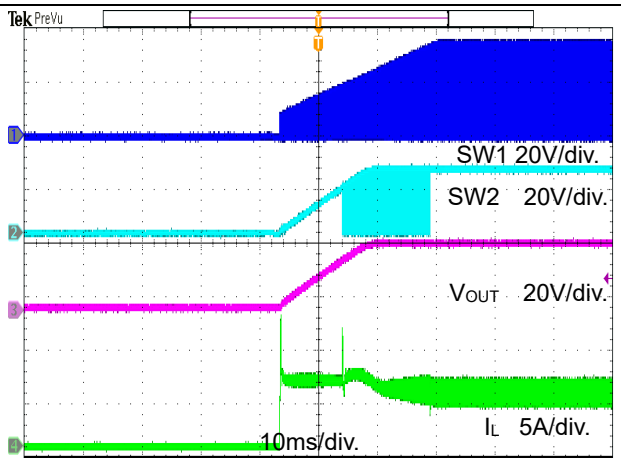


Figure 4. Start Up I_{OUT}=5A CCM

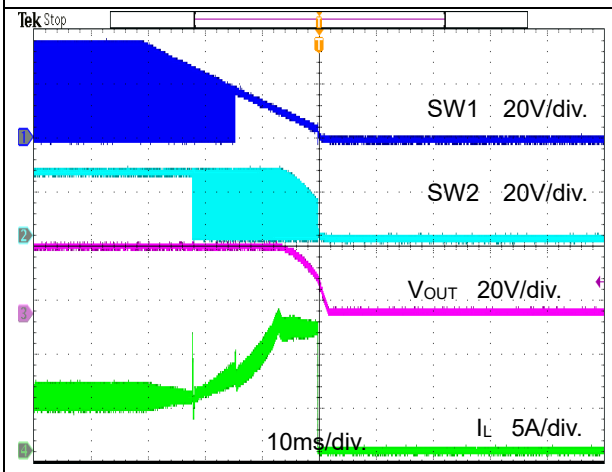


Figure 5. Shut Down Through VIN I_{OUT}=5A

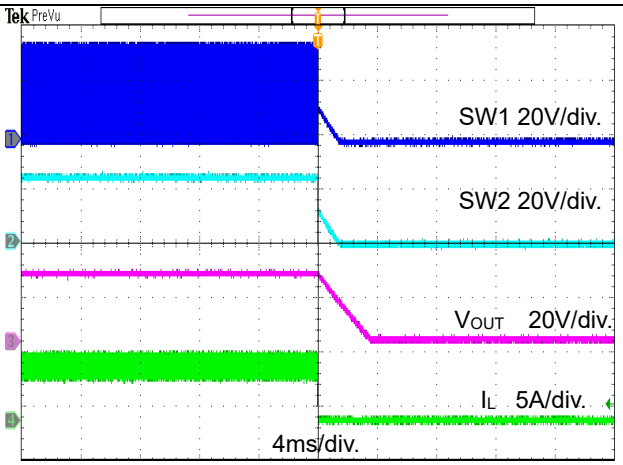


Figure 6. Shut Down Through EN I_{OUT}=5A

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 15V, V_{OUT} = 24V, F_{sw} = 300 kHz, T_J = -40°C to +125°C, unless otherwise noted.

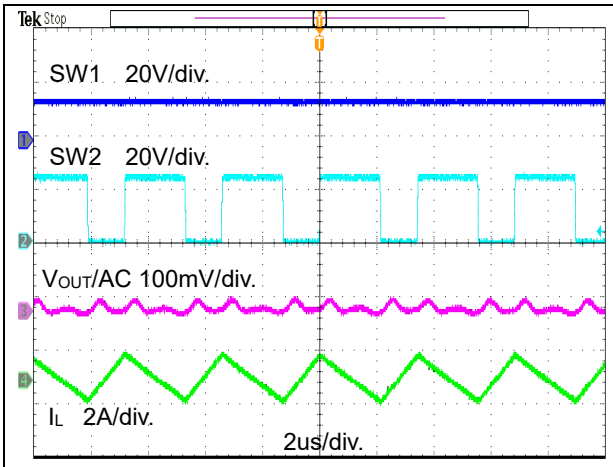


Figure 7. Steady State I_{OUT}=0A CCM

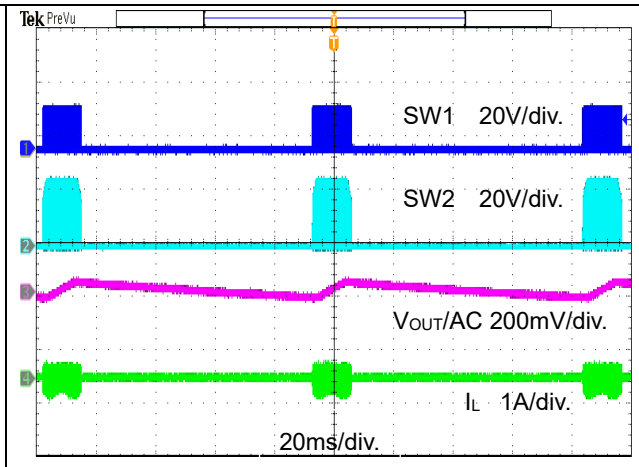


Figure 8. Steady State I_{OUT}=0A DEM

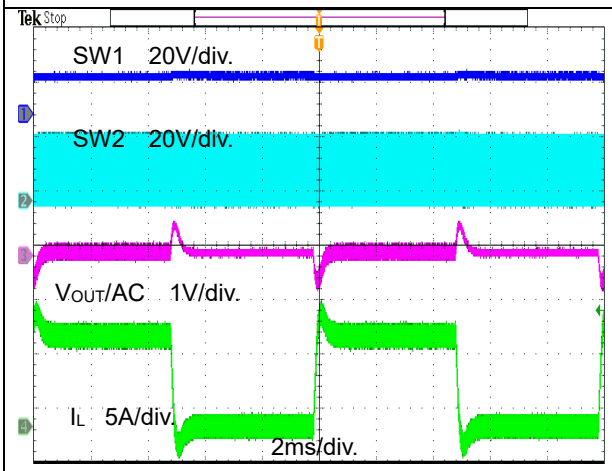


Figure 9. Dynamic Load I_{OUT}=0-5A CCM

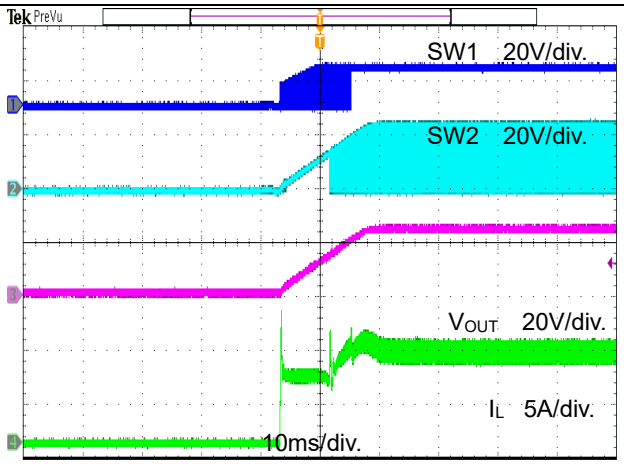


Figure 10. Start Up I_{OUT}=5A CCM

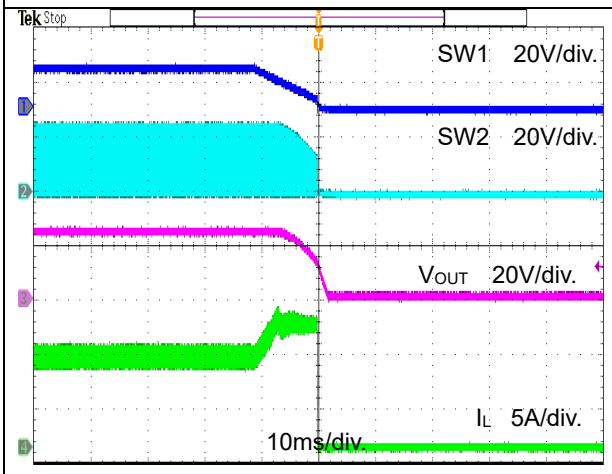


Figure 11. Shut Down Through VIN I_{OUT}=5A

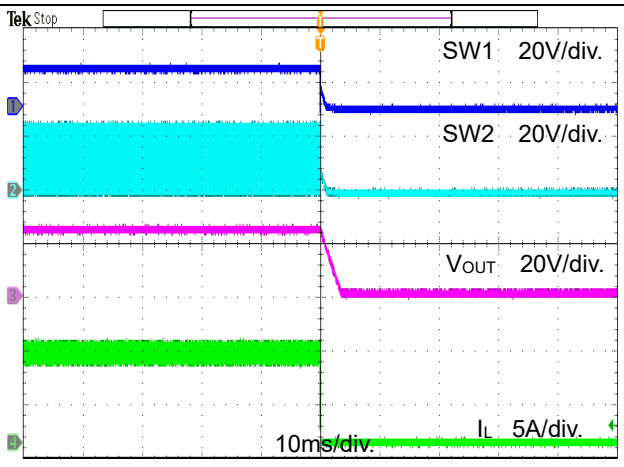


Figure 12. Shut Down Through EN I_{OUT}=5A

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 24V, F_{sw} = 300 kHz, T_J = -40°C to +125°C, unless otherwise noted.

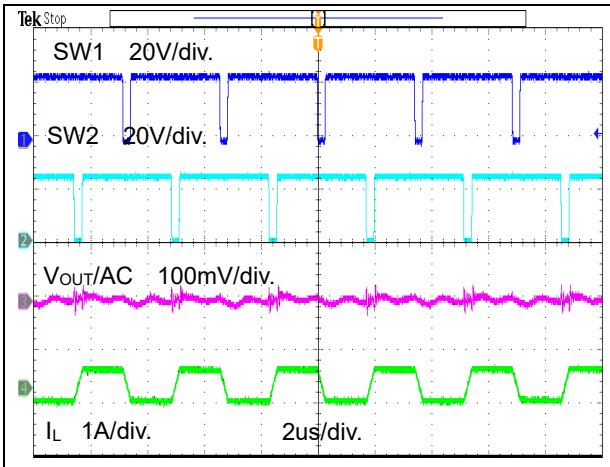


Figure 13. Steady State I_{OUT}=0A CCM

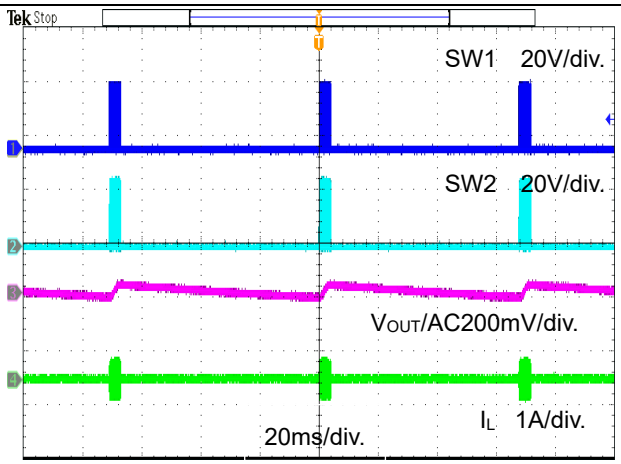


Figure 14. Steady State I_{OUT}=0A DEM

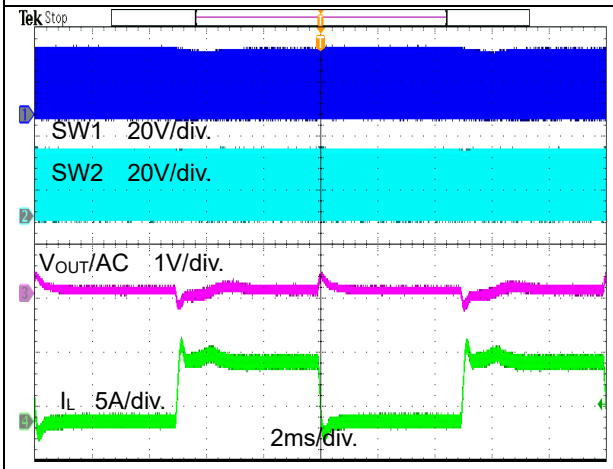


Figure 15. Dynamic Load I_{OUT}=0-5A CCM

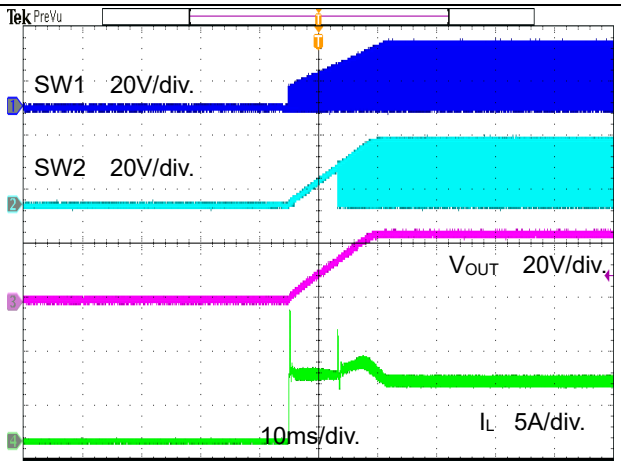


Figure 16. Start Up I_{OUT}=5A CCM

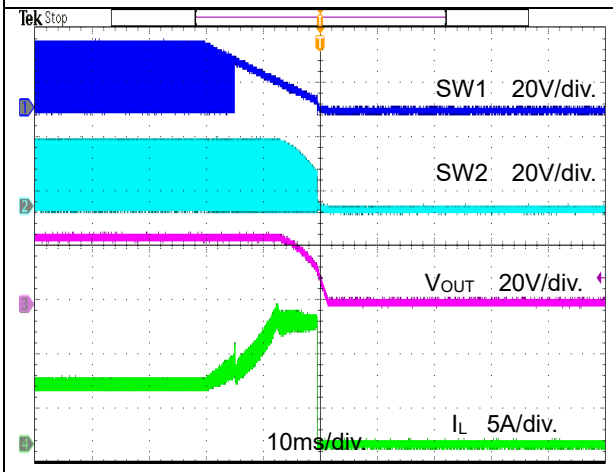


Figure 17. Shut Down Through VIN I_{OUT}=5A

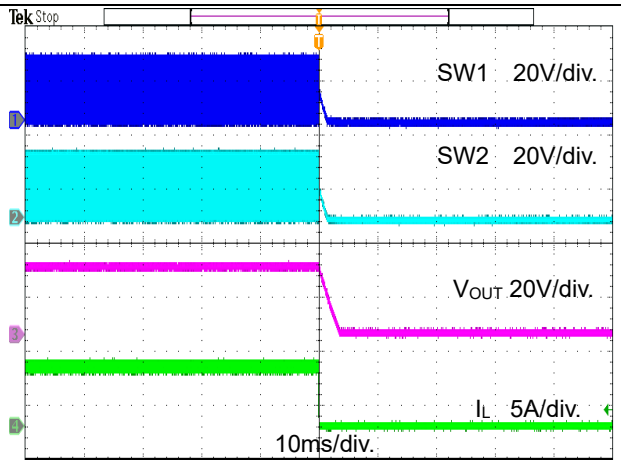


Figure 18. Shut Down Through EN I_{OUT}=5A

FUNCTION DESCRIPTION

Operation

The VE8620 is a current mode 4-switch buck-boost controller that provides an output voltage above, equal to or below the input voltage. The VE8620 uses current mode in buck or boost operation. It operates in buck mode when VIN is greater than VOUT and in boost mode when VIN is less than VOUT. It operates buck-boost mode when VIN is close to VOUT.

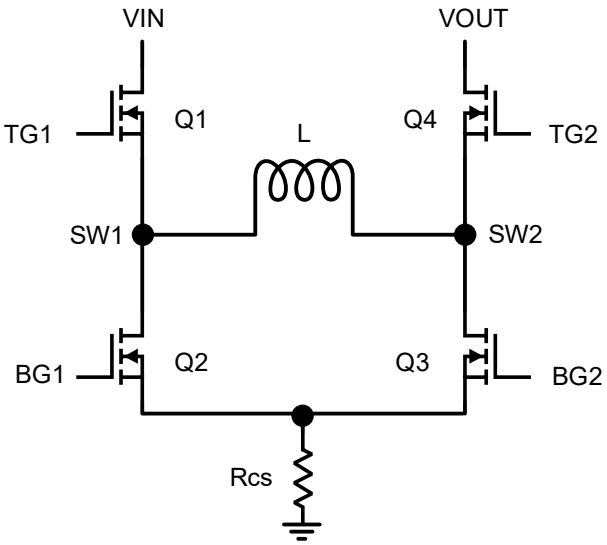


Figure 19. 4 Switch Buck-Boost

Boost Mode

In boost mode switch Q1 is always on and switch Q2 is always off. It operates peak current mode boost as Figure 20, behaving likes a typical synchronous boost regulator.

At the start of every cycle, switch Q3 is turned on first. Inductor current is sensed by Rcs when Q3 is turned on. After the sensed current exceeds the reference voltage, which is proportional to COMP, synchronous switch Q3 is turned off and switch Q4 is turned on for the remainder of the cycle.

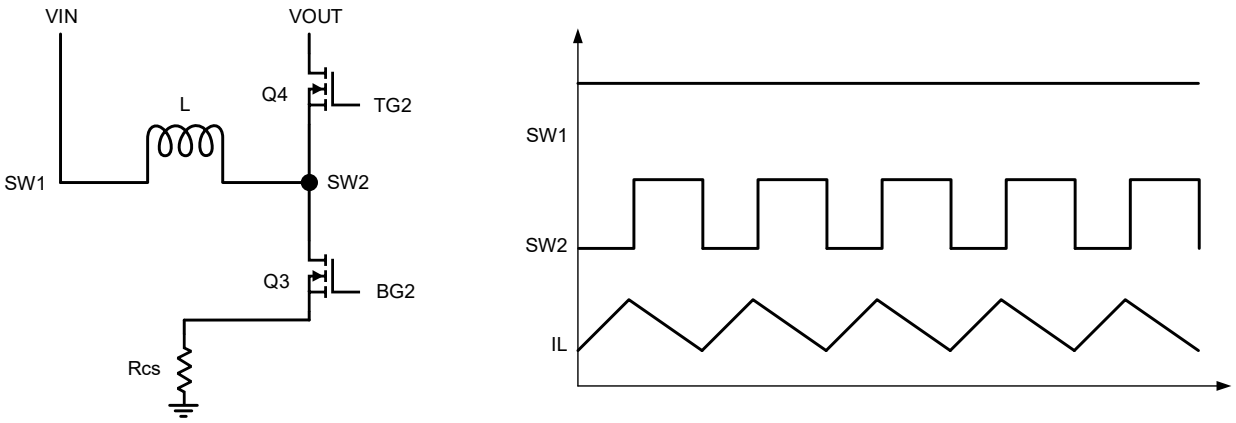


Figure 20. Boost Mode

Buck Mode

In buck mode switch Q4 is always on and switch Q3 is always off. It operates valley current mode buck as Figure 21, behaving likes a typical synchronous buck regulator.

At the start of every cycle, synchronous switch Q2 is turned on first. Inductor current is sensed by Rcs when Q2 is turned on. After the sensed current falls below the reference voltage, which is proportional to COMP, synchronous switch Q2 is turned off and switch Q1 is turned on for the remainder of the cycle.

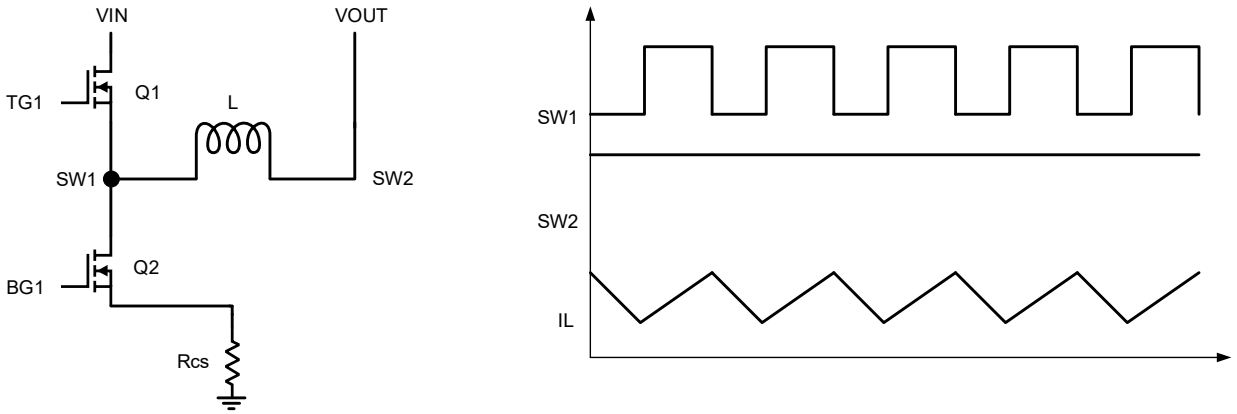


Figure 21. Buck Mode

Buck-boost Mode

VE8620 works in buck-boost mode as Figure 22 when VIN approaches the VOUT. Every cycle VE8620 turns on switches Q2 and Q4, then Q1 and Q4 are turned on until 180° later when switches Q1 and Q3 turn on, and then switches Q1 and Q4 are turned on for the remainder of the cycle.

When VIN is higher than VOUT but close to VOUT,

The VE8620 enters the buck-boost mode when the duty cycle of buck D_{buck} is greater than

D_{bb1} =(T-250ns)/T

Where T is the switching period.

$D_{buck}=Ton_{\_TG1}/T$

It exits from buck-boost mode and return to buck mode when D_{buck} is less than

D_{bb2}=1-(0.25T+200ns)/T

When VIN is lower than VOUT but close to VOUT,

The VE8620 enters the buck-boost mode when the duty cycle of boost D_{boost} is less than

D_{bb3} = 250ns/T

$D_{boost}=Ton_{\_BG2}/T$

It exits from buck-boost mode and return to boost mode when D_{boost} is higher than

D_{bb4} =(0.25T+200ns)/T.

Figure23 shows operating mode vs duty cycle

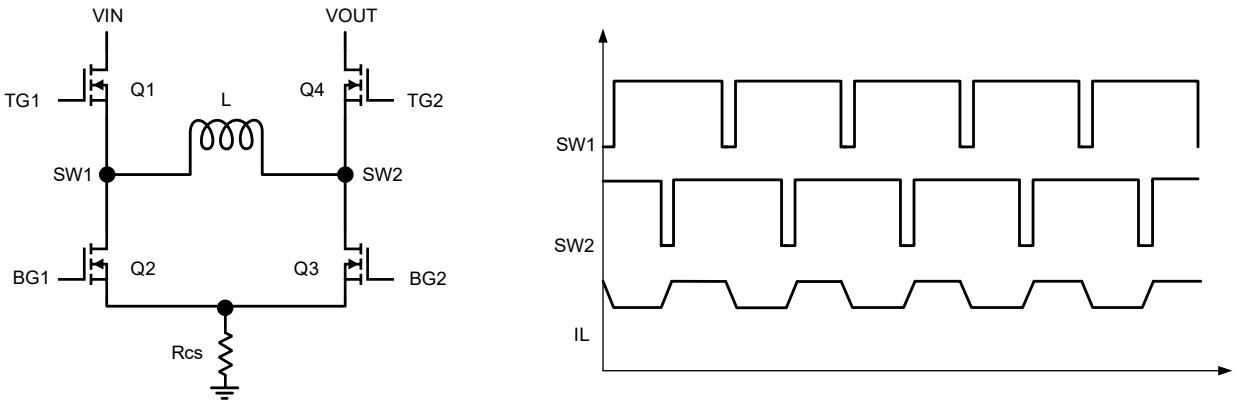


Figure 22. Buck-Boost Mode

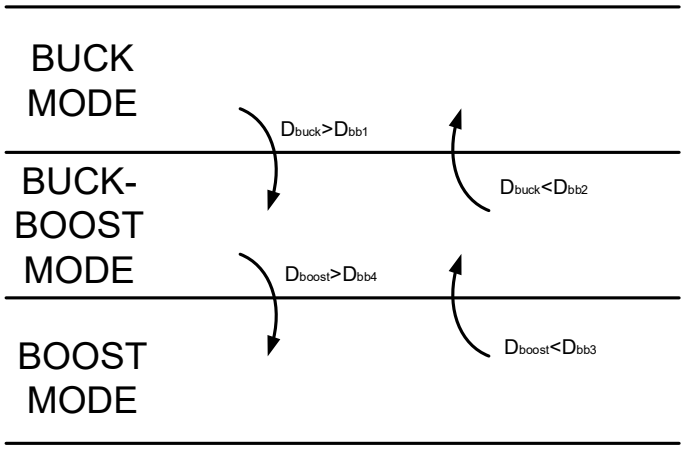


Figure 23. Mode vs Duty Cycle

EN_UVLO

The VE8620 has a dedicated enable (EN_UVLO) control that uses a bandgap - generated precision threshold of 1.2V. By pulling EN_UVLO high or low, the IC can be enabled or disabled.

VCC Regulator Connection

VCC can be powered from both VIN and EXTBIAS. If connecting EXTBIAS to an external power supply, EXTBIAS should be higher than 4.7V but less than 24V. When VIN is less than 5.5V, EXTBIAS should be biased by external source. If V_{OUT} is higher than 5V but less than 24V, EXTBIAS can be connected to V_{OUT} with a resistor or diode. The recommend value of this resistor is 10Ω.

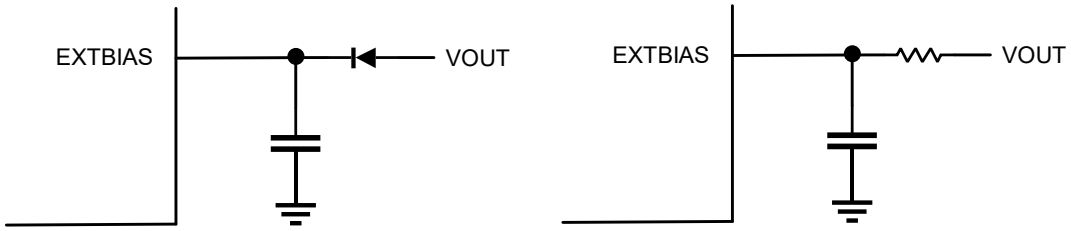


Figure 24. EXTBIAS Connection

Low Current Operation

The VE8620 is recommended to run in forced continuous conduction mode at heavy load by pulling the CCM pin higher than 1.5V. In this mode the controller behaves as a continuous current mode synchronous switching regulator.

However, reverse inductor current from the output to the input is not desired for certain applications. For these applications, the CCM pin must be connected to GND to operate in DCM. In this mode, switch Q4 turns off when the inductor current flows negative.

It also can be pulled low by the C/10 pin when the output current is low as shown in Figure 25. The C_{CCM} is used to adjust the delay time from DCM to CCM.

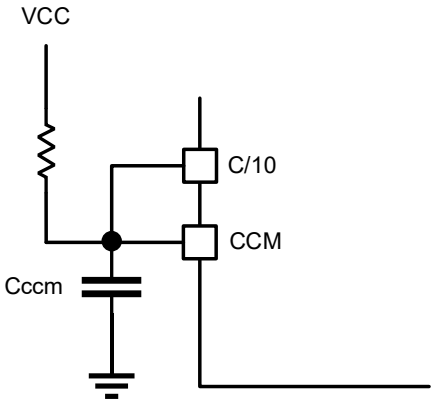


Figure 25. Low Current Operation

Programming Frequency

The VE8620's frequency can be programmed from 100KHz to 700KHz with a resistor from RT to SGND. The Value of R_{RT} can be calculated with Equation (1):

$$R_{RT}(K\Omega) = \frac{1000}{0.0202 \times Fsw(KHz)} - 9 \qquad (1)$$

Frequency Synchronization

The VE8620 switching frequency can be synchronized from 150K to 700K using the SYNC pin. Driving SYNC with a pulse the duty cycle between 10% and 90%. The frequency of external clock must be higher than 70% of the frequency set by RT.

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V to 3V. When it is lower than REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

An external capacitor connected from SS to SGND is charged from an internal 4μA current source, producing a ramped voltage. The soft - start time (T_{SS}) is set by the external SS capacitor and can be calculated by Equation (2):

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(uA)} \qquad (2)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (1.2V), and I_{SS} is the 4μA SS charge current. There is no internal SS capacitor. SS is reset when a fault protection other than OVP or peak current limit occurs.

SHORT Pin

The VE8620 provides an open-drain status pin, SHORT, which pulls low when the FB pin is below 400mV and V_{ISMON} is above 120mV. During start-up the VE8620 ignores the voltage on the FB pin until the soft-start capacitor reaches 1.5V.

C/10 Pin

The VE8620 provides an open-drain status pin, C/10, which pulls low when the voltage V_{ISMON} is less than 100mV. For battery charger applications with output current sense and limit, the C/10 provides a C/10 charge termination flag.

Gate Driver

The low-side gate driver is supplied from VCC. The high-side gate driver is supplied from BST. A boot capacitor connected from the BST to the SW provides power to the high-side MOSFET driver. This floating driver has its own under-voltage lockout (UVLO) protection. This UVLO's rising threshold is 3.6V with a hysteresis of 100mV. If the BST voltage is lower than the bootstrap UVLO, the VE8620 enters boot refresh mode to ensure that the BST capacitor is high enough to drive the HS-FET.

Current Monitor

The VE8620 has two current sense operational amplifiers which can monitor both input and output current when it works on unidirectional mode as shown in Figure 26.

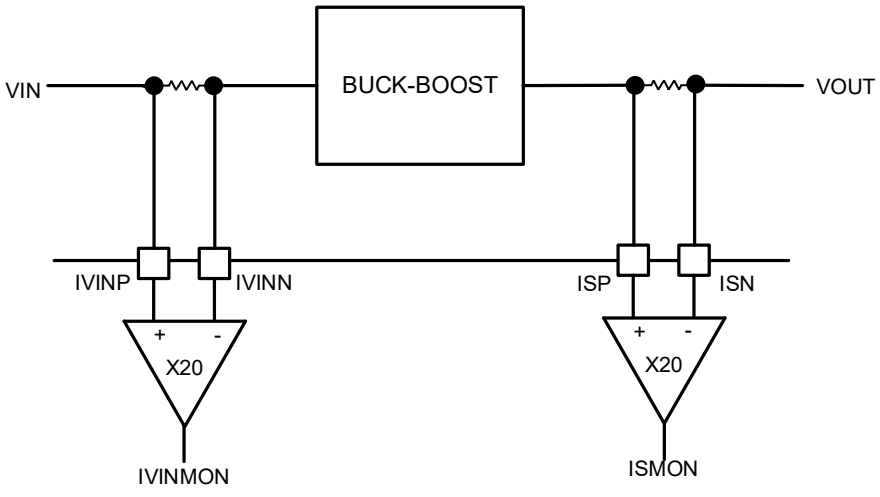


Figure 26. Input and Output Current Monitor

ISMON and IVINMON

The ISMON and IVINMON pins provide a linear indication of the current flowing through the output. The equation for V_{ISMON} and $V_{IVINMON}$ are

$$V_{ISMON} = 20 \times V_{(ISP-ISN)}$$
$$V_{IVINMON} = 20 \times V_{(IVINP-IVINN)}$$

These pins are suitable for driving an ADC input, however, the output impedance of these pins is 80kΩ so care must be taken not to load this pin.

Current Control

The CTRL can be used to adjust the current. When the CTRL voltage is less than 1.1V, the voltage on the ISMON pin is limited to the voltage on the CTRL pin as shown in Figure 27.

When the CTRL pin voltage is between 1.1V and 1.4V the voltage on the ISMONT pin varies with VCTRL. when VCTRL > 1.4V the voltage on the ISMON pin no longer varies.

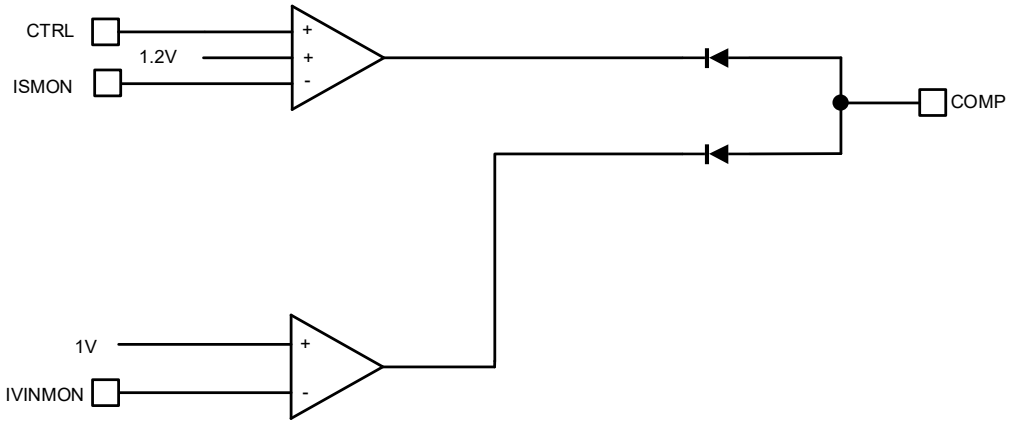


Figure 27. Current Control

Low Side Current Sense

The SNSP and SNSN pins sense the low side current which is used to implement the current mode control and peak valley current limit.

To prevent false triggering due to the switching noise, an RC filter maybe required as shown in Figure 28.

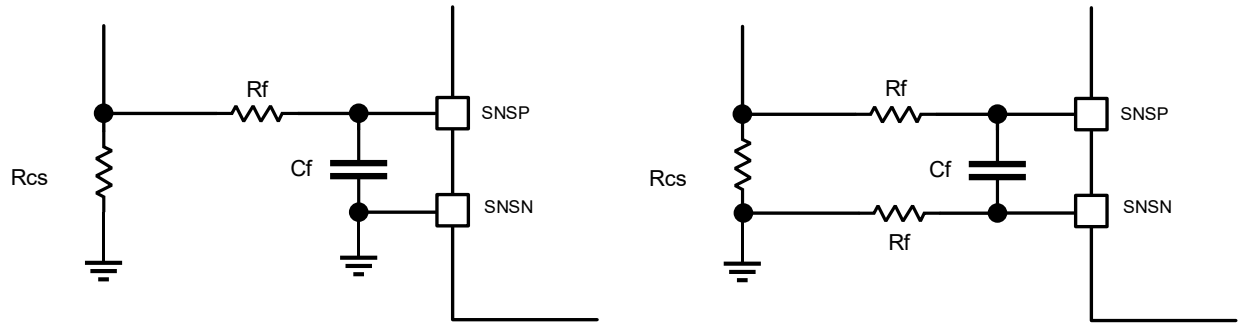


Figure 28. Filter for Low Side Current Sense

Voltage Loop Compensation

The compensation resistor and capacitor at COMP are set to optimize the voltage loop. The typical value of the compensation capacitor is 22n and the value of compensation resistor is 10k. Higher capacitance and lower resistance will improve stability but slow the loop response.

Current Loop Compensation

The filter of current sense will improve the stability of current loop. Connecting a RC filter to IVINN or ISN as shown in Figure 29 if the ripple current on the current sense resistor is large. Do not connect the resistor to IVINP or ISP pin.

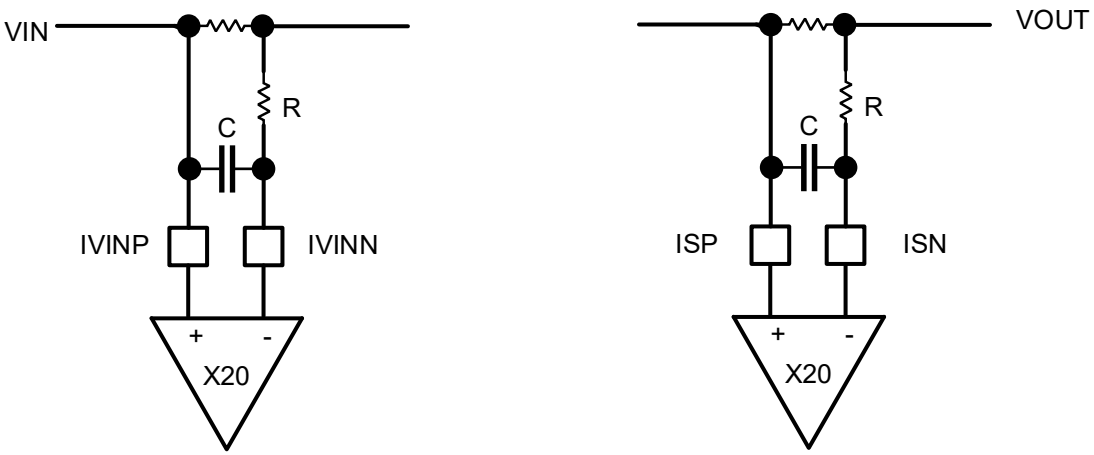


Figure 29. High Side Current Loop Compensation

Another way to filter the current signal is connecting a capacitor to ISMON or IVINMON as shown in Figure 30.

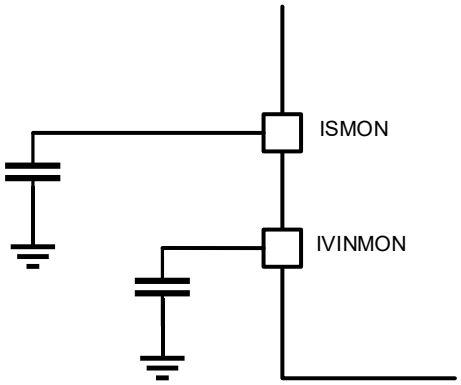


Figure 30. Low Side Current Loop Compensation

PCB Layout Guidelines

1. The PGND ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
2. Place CIN, switch Q1, switch Q2 in one compact area. Place COUT, switch Q3, switch Q4 in one compact area.
3. Keep the high dv/dt SW1, SW2, BST1, BST2, TG1 and TG2 nodes away from sensitive small-signal nodes.
4. The path formed by switch Q1, switch Q2, and the C_{IN} capacitor should have short leads and PC trace lengths. The path formed by switch Q3, switch Q4, and the C_{OUT} capacitor also should have short leads and PC trace lengths.

5. Connect the top driver bootstrap capacitor, C1, closely to the BST1 and SW1 pins. Connect the top driver bootstrap capacitor, C2, closely to the BST2 and SW2 pins.
6. Connect the input capacitors, C_{IN}, and output capacitors, C_{OUT}, closely to the power MOSFETs. These capacitors carry the MOSFET AC current in boost and buck operation.
7. Route SNSN and SNSP leads together with minimum PC trace spacing. Avoid sense lines pass through noisy areas, such as switch nodes. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
8. Connect the COMP pin compensation network close to the IC, between COMP and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
9. Connect the VCC bypass capacitor close to the IC, between the VCC and the power ground pins. This capacitor carries the MOSFET drivers' current peaks.

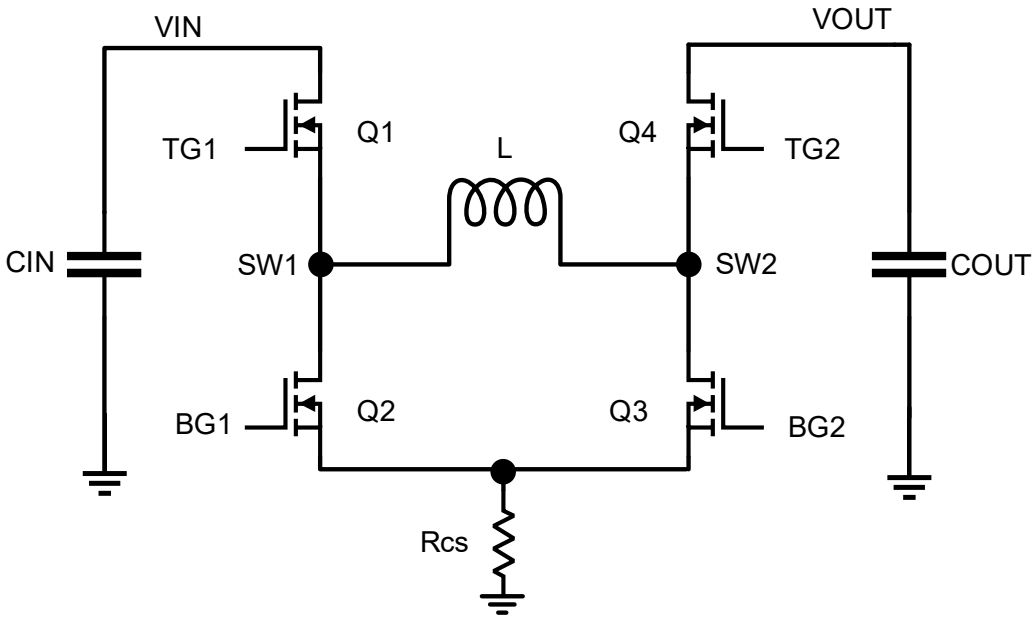
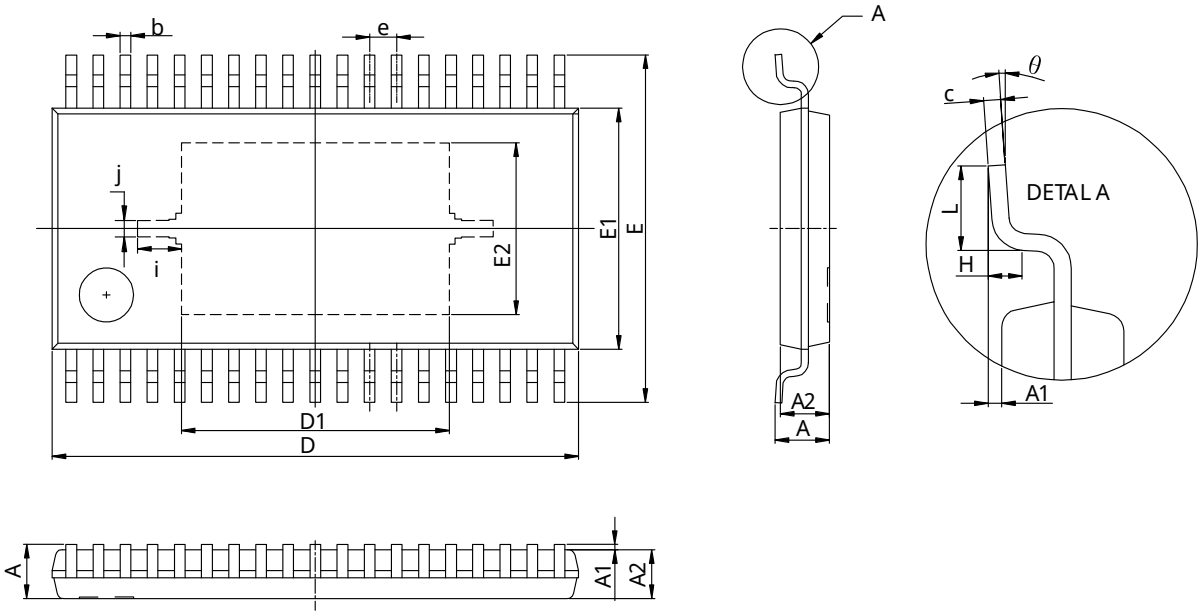


Figure 31. Power Stage of Buck-boost

PACKAGE INFORMATION

TSSOP-38-EP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
D1	4.840	5.040	0.191	0.198
E	6.250	6.550	0.246	0.258
E1	4.300	4.500	0.169	0.177
E2	3.060	3.260	0.120	0.128
e	0.0500(BSC)		0.020(BSC)	
L	0.500	0.700	0.020	0.028
H	0.250(TYP)		0.010(TYP)	
i	0.705	0.905	0.028	0.036
j	0.200	0.400	0.008	0.016
θ	1°	7°	1°	7°

REVISION HISTOR

Revision	Data	Description
1.0	2024-10-15	Initial Release