Configurable Digital Output High-speed Linear Hall

1. Features

- Supports high-speed applications up to 32K
- Integrated ultra-low power mode with wake-up functionality
- Configurable sensitivity and quiescent output
- Supports 8M SPI communication and daisy-chain connection
- Built-in self-test function for rapid key status detection
- Operating voltage range: 3.0V-5.5V
- Integrated 12-bit ADC
- Available in SOT23-6L & DFN2×2-8L PKG types

2. Applications

- Analog magnetic axis keyboards
- Tactile switches
- Magnetic mute switches
- Joystick applications

3. Description

The SC4391 is a linear Hall sensor with wake-up functionality and configurable digital output. It integrates a magnetic sensing element and high-precision ADC module to accurately convert external magnetic field variations into digital signals.

The device features multiple configurable registers that allow adjustment of sensitivity and quiescent output voltage to meet various application requirements. The operating mode can also be configured via registers to satisfy different speed and power consumption needs.

In practical applications, the host can acquire 12-bit ADC digital data through a 4-wire SPI communication protocol. Multiple SC4391 devices can be connected in a daisy-chain configuration for high-speed, high-precision multi-point detection and data transmission.

The SC4391 is available in two package options: DFN2020-8L and SOT23-6L, both featuring 100% lead-free and halogen-free green packaging compliant with environmental requirements.

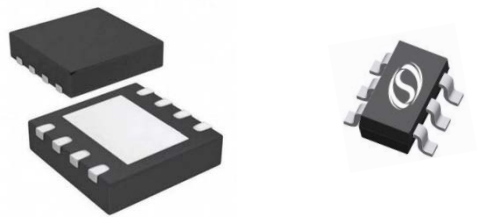

Fig.1 DFN2×2-8L(Left) & SOT23-6L(Right) Package Outline

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4. Terminal Configuration

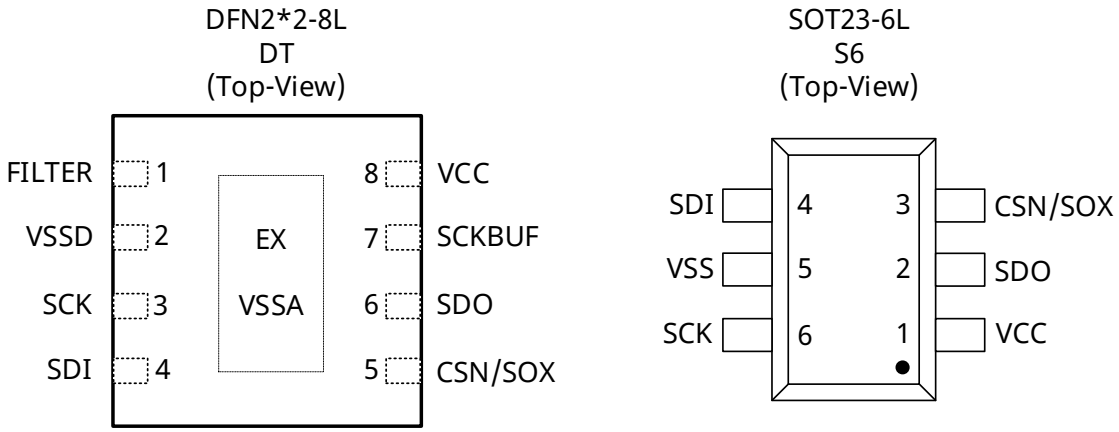


Fig.2 DFN2×2-8L(Left) & SOT23-6(Right) Pin Description

Name	PKG		Pin type	Description
	DFN2*2	SOT23-6		
FILTER	1	1	I/O	Exterior capacitor filter, recommend 4.7nF capacitor
VSSD	2	5	GND	Digital ground terminal
SCK	3	6	I	SPI clock input
SDI	4	4	I	SPI data input
CSN/SOX	5	3	I/O	SPI CSN signal input or SOX output
SDO	6	2	O	SPI Data output
SCKBUF	7		O	SCK buffered output, can be configured by register
VCC	8		PWR	Power supply
VSSA	EX		GND	Analog ground terminal

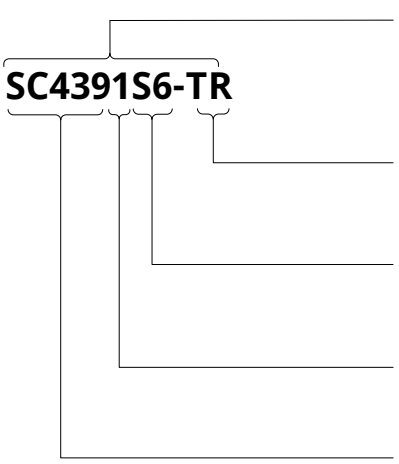
5. Ordering Information

Ordering Information	Sens(mV/Gs) (1)	Ambient, T_A(℃)	Package	Packing	Quantity
SC4391S6-TR	2.4~8.6	-40-85	SOT23-6L	TR	3000/Reel
SC4391DT-TR	2.4~8.6	-40-85	DFN2*2-8L	TR	3000/Reel

Note:

(1) This sensitivity data is available under 3.3v application conditions

Order information format description



Part Number

Pack Designation
TR: Tape & Reel

Package Designation
S6: SOT23-6L
DT: DFN2*2-8L

Magnetic Parameter
Different sensitivity

Device Family
SC439: Configurable digital output high-speed linear Hall

6. Absolute Maximum Ratings

Symbol	Parameter	Notes	Min.	Max.	Units
VCC	Supply voltage	B = 0mT, T_A = 25°C	-0.3	6	V
SDO,CSN	Output voltage	B = 0mT, T_A = 25°C	-0.3	6	V
SCK,SDI,SOX	Input voltage	B = 0mT, T_A = 25°C	-0.3	6	V
T_A	Operating temperature		-40	85	℃
T_J	Junction temperature		-55	165	℃
T_{STG}	Storage temperature		-65	175	℃

Note：
Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7. ESD Protection

Symbol	Parameter	Test conditions	Min.	Max.	Units
V_{ESD_HBM}	HBM	Refer to ANSI/ESDA/JEDEC JS-001 standard(1)	-4	4	kV

Note：
(1) HBM testing follows the AEC-Q100-002 standard.

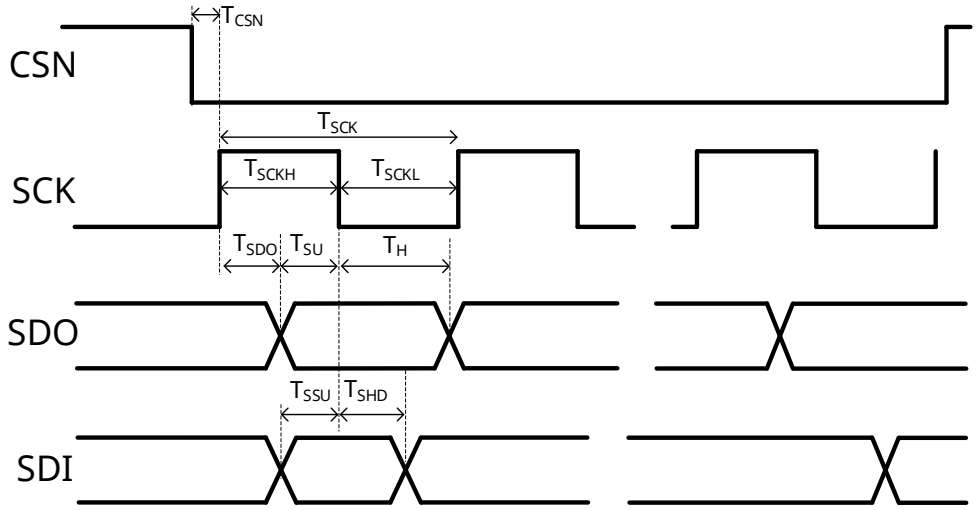
8. Operating Characteristics

（Operating voltage: 3.3V, ambient temperature: 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Umit
V_{CC}	Operating voltage	$T_J < T_{J(Max.)}$	3	3.3	5.5	V
I_{CC}	Average operating current	$f_{SCANNING}$ =4kHz，$t_{SETTING}$=2μs，n_{ADC}=4	-	0.8	-	mA
I_{LP}	Low-power mode average current	t_{LP}=50mS	-	2	-	μA
t_{LP}	Ultra-low-power scan interval		-	50	-	ms
V_{UVLO}	Undervoltage lockout threshold	VCC drops below this value, SPI reports Fault	-	2.3	-	V
f_{OSC}	Internal clock	CFG_OSC32M register	-	32	-	MHz
$f_{SCANING}$	Keyboard data scan frequency	CFG_SCAN register: 00	-	32	-	kHz
		CFG_SCAN register: 01	-	16	-	
		CFG_SCAN register: 10	-	8	-	
		CFG_SCAN register: 11	-	4	-	
$t_{SETTING}$	Analog signal settling time	4-bit configurable (2μs~80μs, see register table)	2	-	80	μs
f_{ADCCLK}	ADC sampling clock	CFG_ADCSCK register: 0=16MHz; 1=8MHz	-	8/16	-	MHz
n_{ADC}	ADC sampling count	CFG_ADCNUM register: 00	-	1	-	times
		CFG_ADCNUM register: 01	-	2	-	
		CFG_ADCNUM register: 10	-	4	-	
		CFG_ADCNUM register: 11	-	8	-	
$t_{ADCSAMP}$	Single ADC sampling time	ADC clock = 16MHz	-	1.5	-	μs
V_{SENSC}	Sensitivity coarse adjustment range	3-bit configurable (CFG_SCOARSE register)	2.4	-	8.6	mV/Gs
V_{S_STEP}	Sensitivity coarse adjustment step		-	20	-	%
V_{SENSF}	Sensitivity fine adjustment range	5-bit configurable (CFG_SFINE register)	0	-	25	%
V_{S_STEP}	Sensitivity fine adjustment step	LSB step	-	0.78	-	%
POL_{DFN}	Polarity (DFN package)	CFG_POL register: 0	-	S	-	-
		CFG_POL register: 1	-	N	-	-
POL_{SOT23}	Polarity (SOT23 package)	CFG_POL register: 0	-	N	-	-
		CFG_POL register: 1	-	S	-	-
V_{QC}	Quiescent output voltage coarse range	CFG_VQSET register: 0	-	3890	-	LSB
		CFG_VQSET register: 1	-	2048	-	LSB
V_{QF}	Quiescent output voltage fine range	6-bit configurable (CFG_VQFINE register)	-500	-	500	LSB
V_{QF_STEP}	Quiescent output voltage ADJ step	LSB step	-	18	-	LSB

9. SPI Transmission Characteristics

（The SC4391 supports a 4-wire slave SPI interface, outputs data on the rising edge, samples data on the falling edge, and supports full-duplex data transmission with an 8-bit data width.）



Symbol	Parameter	Min	Typ	Max	Unit
SPI timing parameter					
T_{CSN}	CSN setup time	20	-	-	ns
T_{SCKH}	CLK high level time	40	-	-	ns
T_{SCKL}	CLK low level time	40	-	-	ns
T_{SCK}	CLK cycle time limit	60	-	-	ns
T_{SSU}	SDI setup time	10	-	-	ns
T_{SHD}	SDI hold time	10	-	-	ns
T_{SDO}	SDO output delay	-	-	20	ns
T_{SU}	SDO setup time	10	-	-	ns
T_{H}	SDO hold time	4	-	-	ns
SPI electric parameter					
V_{IH}	Input threshold voltage high	-	-	2	V
V_{IL}	Threshold voltage low	0.8	-	-	V
VIN_{HYS}	Hysteresis	-	0.5	-	V
V_{OH}	Output voltage low	$0.8*V_{CC}$	-	-	V
V_{OL}	Output voltage high	-	-	$0.2*V_{CC}$	V

10. Block Diagram

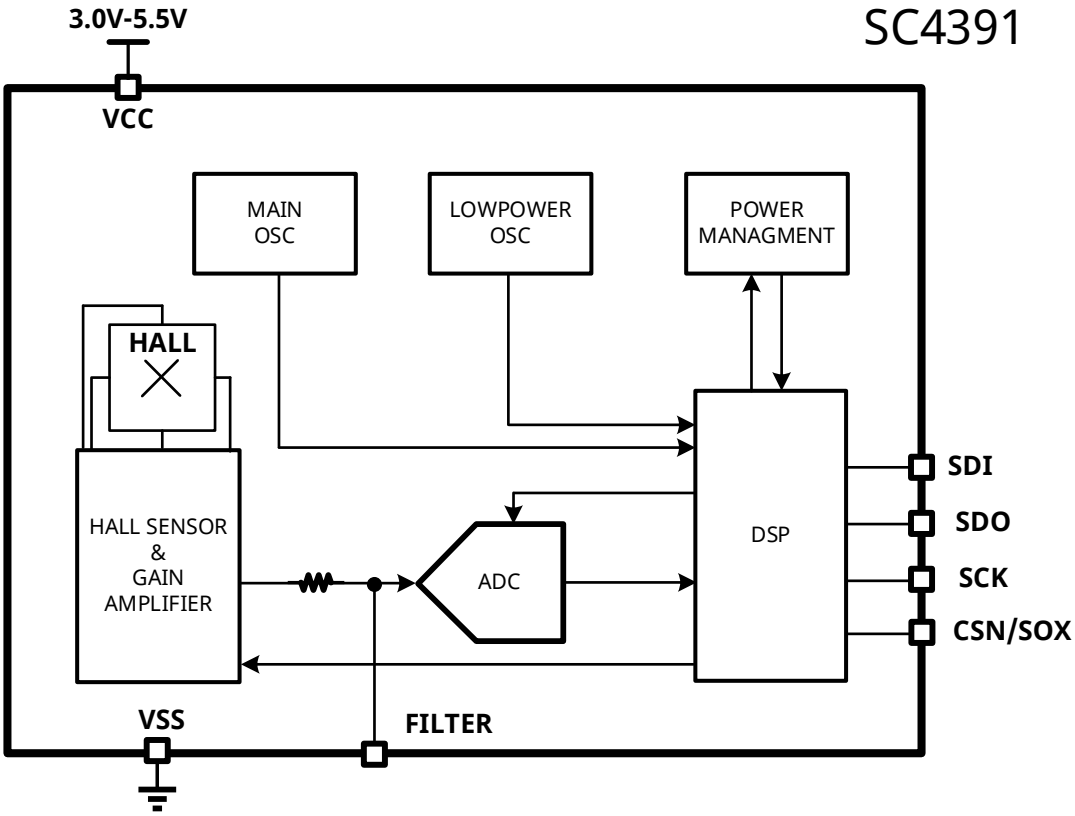


Fig.3 Block Diagram

11. Function Description

Communication Protocol: The SC4391 supports two communication modes: command mode and SPI mode.

No.	Operating Mode	Entry Condition
1	Normal mode	SCK duty cycle >25% (typically 50%)
2	Ultra-low-power mode	SCK high-level time >100μs
3	Self-test mode	Three consecutive SCK duty cycles <25%

Under SPI model, use CSN, SCK, SDI, and SDO pins. SCK serves as the register shift clock. To distinguish command protocol from normal read/write clocks, the SCK frequency must be within 4–8MHz. Data is output on the rising edge and sampled on the falling edge.

12. Typical Application

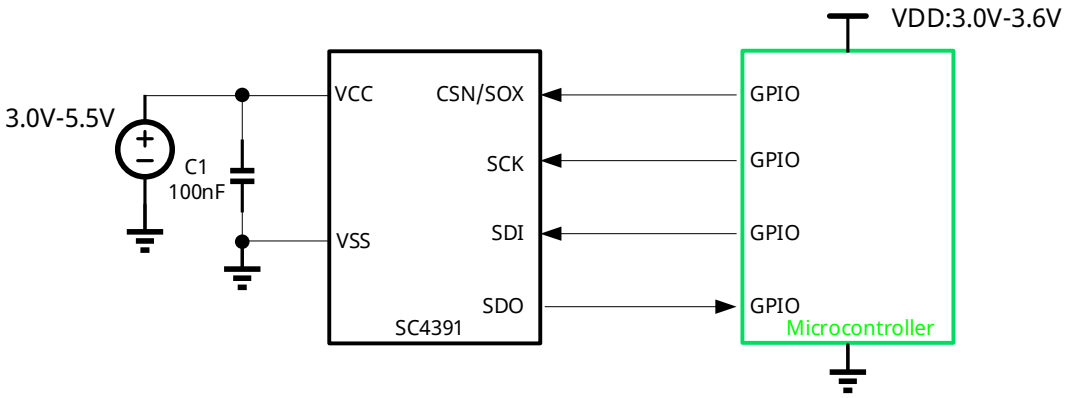
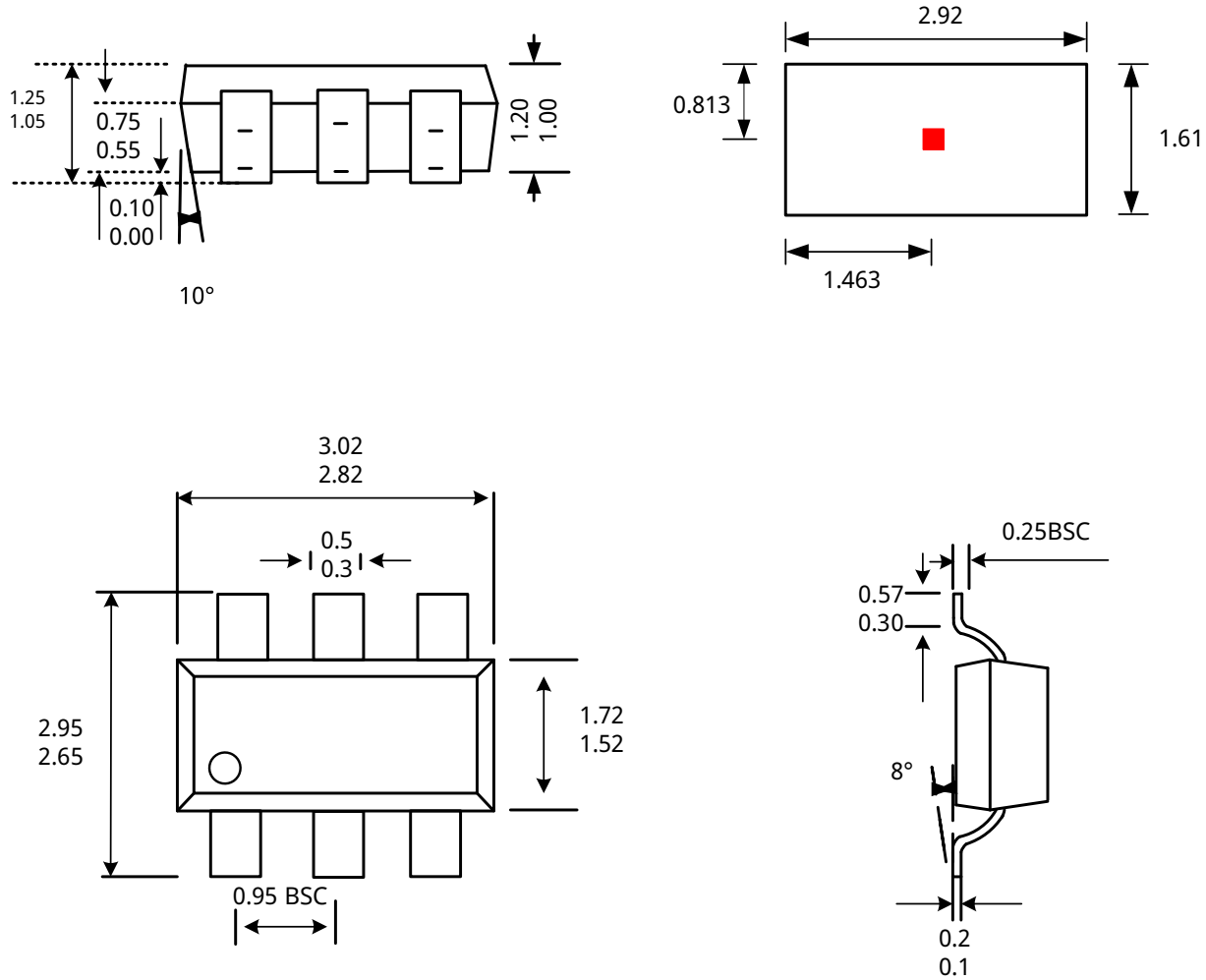


Fig.4 Typical Application Circuit

13. Package Information "SOT23-6L(S6)"

6-PIN
SOT23-6
Package

Unit：mm



Notes:

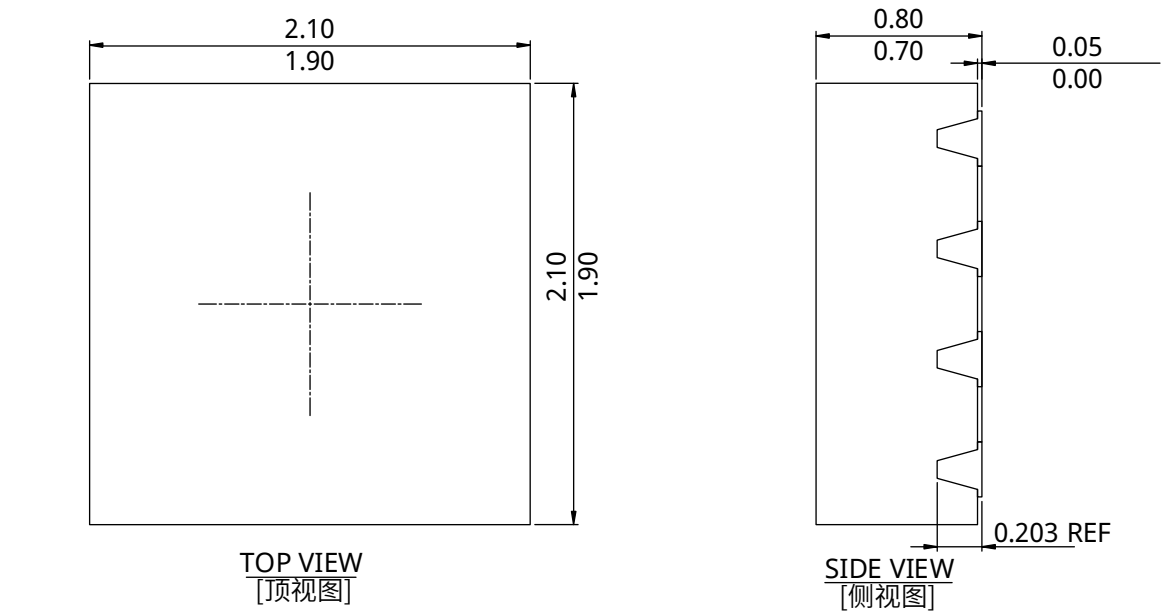
1. *Exact body and lead configuration at vendor's option within limits shown.*
2. *Height does not include mold gate flash.*

Where no tolerance is specified, dimension is nominal.

14. Package Information “DFN2*2-8L(DT)”

8-PIN
DFN2*2-8L
Package

Unit：mm



Notes:

1. *Exact body and lead configuration at vendor’s option within limits shown.*
2. *Height does not include mold gate flash.*

Where no tolerance is specified, dimension is nominal.

15. Revision History

Revision	Date	Description
Rev.E0.1	2024-06-02	Preliminary datasheet
Rev.A1.0	2025-04-01	Unified datasheet format