Square、PWM、AK Protocol Two-Wire Differential Speed Sensor IC

1. Features

- AEC-Q100 Grade0 qualified.
- ISO26262 ASILB certification
- Two-wire current output interface
- Detect speed and direction
- Square wave, PWM and AK protocol outputs
- Fixed, adaptive hysteresis type
- Support vibration suppression
- Support South Pole and North Pole back magnetism
- -40℃ to 150℃ operating temperature range
- Single-chip solution, PCB_Less
- Package：TS-2,TS-2A

2. Product Application

- ABS wheel speed sensor
- Speed sensor

3. Description

The SC968X is an integrated active magnetic sensor based on Hall technology, suitable for wheel speed detection in ABS control systems and iTPMS systems. Its basic function is to measure the speed and direction of magnetic wheels or ferromagnetic gears. Two-wire current interface, with communication via square wave, PWM or AK protocols. It has two types of hysteresis: hidden fixed hysteresis and visible adaptive hysteresis (fine-tuning option). The outstanding sensitivity and accuracy, as well as a wide operating temperature range and other features, make this sensor highly suitable for the demanding requirements of automobiles. The SC968X adopts a PCB_Less package and is equipped with a built-in 2.2nF capacitor, featuring excellent anti-electromagnetic interference capability.

The chip adopts the TS-2/2A packaging form, is matte tin-plated, and uses halogen-free green materials to meet environmental protection requirements.

TS-2

TS-2A

Fig.1 Package Outline

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4. Terminal Configuration

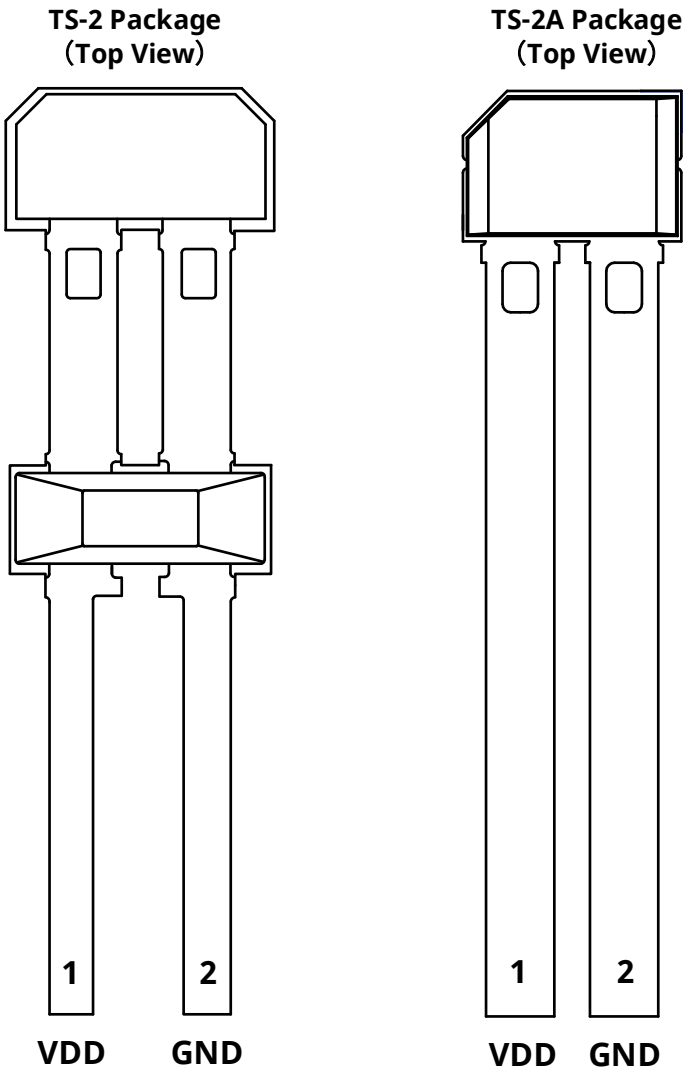


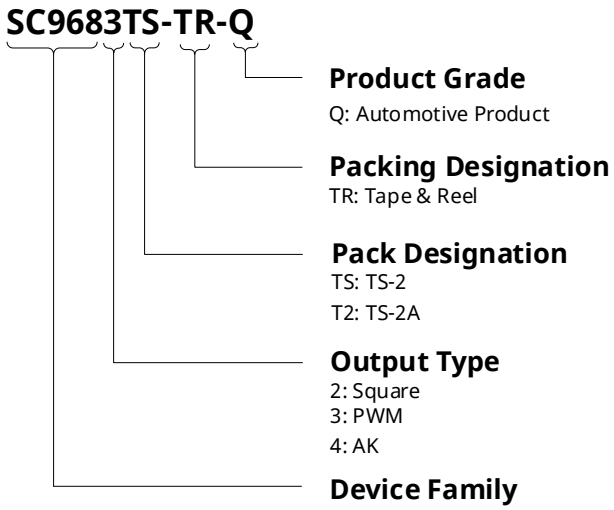
Fig.2 Pin Description

Terminal		Type	Description
Name	Number		
VDD	1	PWR	5.3V to 24V power supply
GND	2	Ground	Ground

5. Ordering Information

Ordering Information	Marking	Output	Ambient, T_A(℃)	Package	Packing	Quantity
SC9682TS-TR-Q	9682	Square	-40 ~ 150	TS-2	Tape & reel	1500pcs/reel
SC9683TS-TR-Q	9683	PWM	-40 ~ 150	TS-2	Tape & reel	1500pcs/reel
SC9683T2-TR-Q	9683	PWM	-40 ~ 150	TS-2A	Tape & reel	1500pcs/reel
SC9684TS-TR-Q	9684	AK	-40 ~ 150	TS-2	Tape & reel	1500pcs/reel
SC9684T2-TR-Q	9684	AK	-40 ~ 150	TS-2A	Tape & reel	1500pcs/reel

Ordering Information Format



6. Absolute Maximum Ratings

Symbol	Parameter	Test conditions	Min.	Max.	Units
V_{DD}	Power supply voltage	Tj=170℃	-	16.5	V
		T=150℃	-	20	V
		t=10 X 5min	-	22	V
		t=10 X 5min, R_M≥75Ω included in V_{DD}	-	24	V
		t=400ms, R_M≥75Ω included in V_{DD}	-	27	V
V_{DDR}	Power supply reverse Voltage	t＜1h, R_M≥75Ω included in V_{DD}	-18	-	V
I_{rev}	Reverse current	t＜4h, R_M≥75Ω included in $V_{DD,}$ external current limitation	-	100	mA
		t＜1h, R_M≥75Ω included in $V_{DD,}$ external current limitation	-	200	mA
T_J	Maximum junction temperature	5000h, V_{DD}＜16.5V, R_M≥75Ω included in V_{DD}	-	150	℃
		500h, V_{DD}＜13V, R_M≥75Ω included in V_{DD}	-	160	℃
		1h, V_{DD}＜13V, R_M≥75Ω included in V_{DD}	-	170	℃
T_{STG}	Storage Temperature		-65	175	℃
R_{thJA}	Thermal resistance	Refer to JESD51-1 standard	-	190	℃/W

Note：
Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7. ESD Protection

Symbol	Parameter	Test conditions	Min.	Max.	Units
V_{ESD_HBM}	HBM	Refer to AEC-Q100-002E HBM standard, R=1.5kΩ, C=100pF	-8	8	kV
V_{ESD_CDM}	CDM	Refer to AEC-Q100-011C CDM standard	-750	750	V

8. Operating Characteristics

8.1 Operating Range

over operating free-air temperature range (V_{DD}=12V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DD}	Operating voltage	Square and PWM	5.3	12	20	V
		AK protocol	6.5	12	20	V
V_{AC}	Supply voltage ripple	V_{DD}=13V, 0＜f_{mod}＜150KHz	-	-	6	Vpp
V_{res_PWM}	Reset voltage	Square and PWM output, reset voltage	3.6	-	4.1	V
V_{rel_PWM}	Return voltage	Square and PWM output, return voltage	4.7	-	5.3	V
V_{res_AK}	Reset voltage	AK protocol output, reset voltage	4.0	-	4.5	V
V_{rel_AK}	Return voltage	AK protocol output, return voltage	5.8	-	6.5	V
dT_{j_Dir}	Temperature change per magnetic period for valid DR	Valid for △B_{dir}＞1.9mT	-7.5	-	7.5	K
dT_{j_Speed}	Temperature change at standsill	Valid for △B＞3mT	-150	-	150	K
△$B_{stat,l/r}$	Pre induction offset between outer probes	B_{left}-B_{right} when the gear is stationary	-30	-	30	mT
△$B_{stat,m/o}$	Pre-induction offset between mean of outer probes and center probe	B_{center}-B_{right} when the gear is stationary	-30	-	30	mT
△B	Differential induction	B_{left}-B_{right} when the gear is rotating	-120	-	120	mT
f_{mag}	Signal frequency		0	-	12	KHz
f_{dir_min}	Minimum magn. frequency for direction detection		-	0	1	Hz

8.2 Electrical Characteristics

over operating free-air temperature range (V_{DD}=12V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{Low}	Supply current low		5.9	7.0	8.4	mA
I_{Mid}	Supply current mid		11.8	14.0	16.8	mA
I_{High}	Supply current high		23.6	28.0	33.6	mA
	Supply current @ V_{res_min}＜V_{DD}		1	-	-	mA
I_{Fault}	ASIL alarm current		1.5	3.5	3.9	mA
dI_X/dV_{DD}	Line regulation		-	-	90	uA/V
t_r，t_f	Current slew rate	10% and 90% value，R_M=50Ω T_j＜170℃	6	-	26	mA/us
t_{d_input}	Initial calibration delay time	Additive to power up time	-	220	300	us
t_{PO}	Power-on time		-	-	1	ms
n_{start}	Number of pulses required for initial offset calibration		-	-	3	edges
$n_{DZ\text{-}Startup}$	The number of edges in uncalibrated mode		-	-	4	edges
n_{supp}	Number of pulses suppressed		-	-	1	pulses
$n_{DZ\text{-}Start}$	Magnetic edges suppressed until output switching		1	-	2	edges
n_{LM}	Number of pulses required for initial LM measurement		3	-	4	pulses
$n_{DR\text{-}Start}$	Number of pulses required for initial valid direction detection	4th pulse has valid direction information $\triangle B_{dir} \geq 2*\triangle B_{limit}$	-	-	4	pulses
n_{DR_change}	Valid direction after change of direction	2nd pulse has valid direction information $\triangle B_{dir} \geq 4*\triangle B_{limit}$	-	-	2	pulses
		6th pulse has valid direction information $\triangle B_{dir} \geq 2*\triangle B_{limit}$			7	pulses
$f_{dir\text{-}limit}$	Frequency limit for direction information availability		-	-	2700	Hz
$S_{jit\text{-}close}$	Jitter-close	△B≥2mT，1sigma，T≤150℃，f=1kHz	-0.7	-	0.7	%
		△B≥2mT，1sigma，T≤170℃，f=1kHz	-2	-	2	%
$S_{jit\text{-}far}$	Jitter-far	2mT≥△B≥$\triangle B_{limit}$，1sigma，T≤150℃，f=1kHz	-2	-	2	%
		2mT≥△B≥$\triangle B_{limit}$，1sigma，T≤170℃，f=1kHz	-4	-	4	%
$S_{jit\text{-}AC}$	Jitter @ board net ripple	V_{DD}=13V±6Vpp，1sigma，0＜f_{mod}＜150kHz △B=15mT	-0.5	-	0.5	%
$S_{jit\text{-}speed}$	Speed pulse jitter	rising edge of speed pulse relative to magnetic edge change	0	-	0.7	us
	Systematic phase error of output edges during start-up and uncalibrated mode		-90	-	90	°
SC9684(AK Protocol)						
t_p	Pulse width for speed pulse		42.5	50.0	57.5	us
t_p	Pulse width for data bits		42.5	50.0	57.5	us

t_{stop}	Standstill time		127.5	150.0	172.5	ms
$t_p/2$	Pulse width $t_p/2$ for initial bit		20	25	30	us
$t_{p\_Bit\_Supp}$	Pulse width t_p for time output offset due to bit stump suppression		42.5	50.0	57.5	us
SC9683 (PWM Protocol)						
$t_{pre-low}$	Pulse width for Output delay		38	45	52	us
$t_{warning}$	Pulse width for alarm mode		38	45	52	us
t_{DR-L}	Pulse width for DR-L		76	90	104	us
t_{DR-R}	Pulse width for DR-R		153	180	207	us
$t_{DR-L\&EL}$	Pulse width for DR-L & EL		306	360	414	us
$t_{DR-R\&EL}$	Pulse width for DR-R & EL		616	720	828	us
$f_{EL,\ max}$	Switching frequency between DR & EL		-	117	-	Hz
t_{stop}	Pulse width for zero velocity		1.232	1.44	1.656	ms
T_{stop}	Pulse period for zero velocity		590	737	848	ms
SC9682(Square Protocol)						
Duty	Duty Cycle	V_{DD}=12V，△B＞2mT，sine wave	40	50	60	%

8.3 Magnetic Properties

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$\triangle B_{limit}$	Limit threshold		0.53	0.75	0.97	mT
$\triangle B_{limit\_drift}$	Limit threshold drift		-5	-	3	%
$\triangle B_{LR}$	Limit range Bit		1.02	1.60	2.18	mT
$\triangle B_{LR\_drift}$	Limit range bit drift		-5	-	3	%
$\triangle B_{LR}/\triangle B_{limit}$	Ratio $\triangle B_{LR}/\triangle B_{limit}$		1.7	2.0	2.5	
$\triangle B_{start\_up}$	The differential magnetic field change amount required for detecting the magnetic field edge in the non-calibration mode (during startup)	Option 00	0.53	0.75	0.97	mT_{pk-pk}
		Option 01	1.22	1.50	1.78	mT_{pk-pk}
		Option 10	2.14	2.50	2.86	mT_{pk-pk}
		Option 11	4.44	5.00	5.56	mT_{pk-pk}
HYS_{min}	Minimum hysteresis threshold of the speed channel	Option 0	0.53	0.75	0.97	mTpkpk
		Option 1	1.22	1.5	1.78	mTpkpk
$HYS_{adaptive}$	Speed channel adaptive hysteresis threshold	Option 0	-	12.5	-	%
		Option 1	-	25	-	%
LM=0	Signal amplitude	99% criteria，according to AK	<0.8	<=1	<=1.2	
LM=1			>0.8	>1	>1.2	
LM=2			>1.48	>1.75	>2.1	
LM=3			>2.5	>2.95	>3.6	
LM=4			>4.2	>4.95	>6	
LM=5			>7	>8.25	>9.9	
LM=6			>12	>14.2	>17.1	
LM=7			>21	>24.7	>29.7	

9. Block Diagram

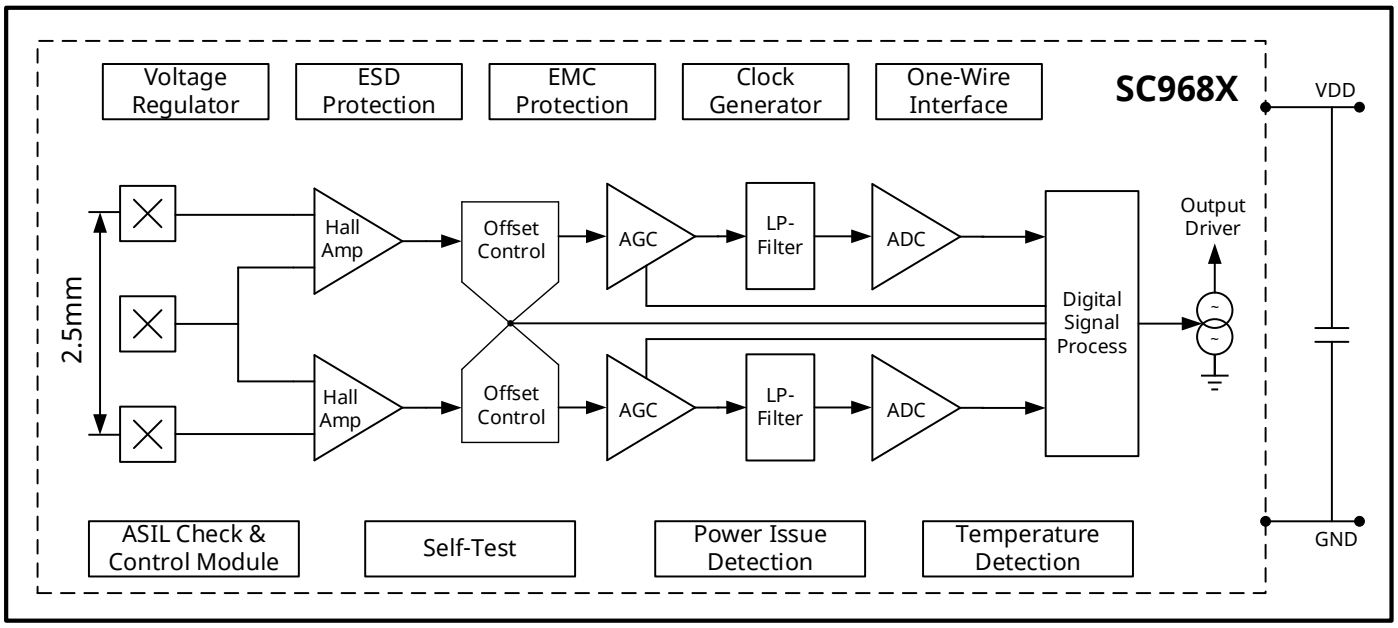


Fig.3 Block Diagram

10. Function Description

10.1 AK Protocol Description

The protocol consists of a start bit, a speed pulse and nine data information bits (data protocol). The data protocol uses Manchester encoding. This means that the value of a bit is encoded by the change in current (I_{mid}) and low current (I_{low}) within a certain time window. "0" is represented by the transition from mid current to low current, and "1" is represented by the transition from low current to mid current. The unused bits are output as default values.

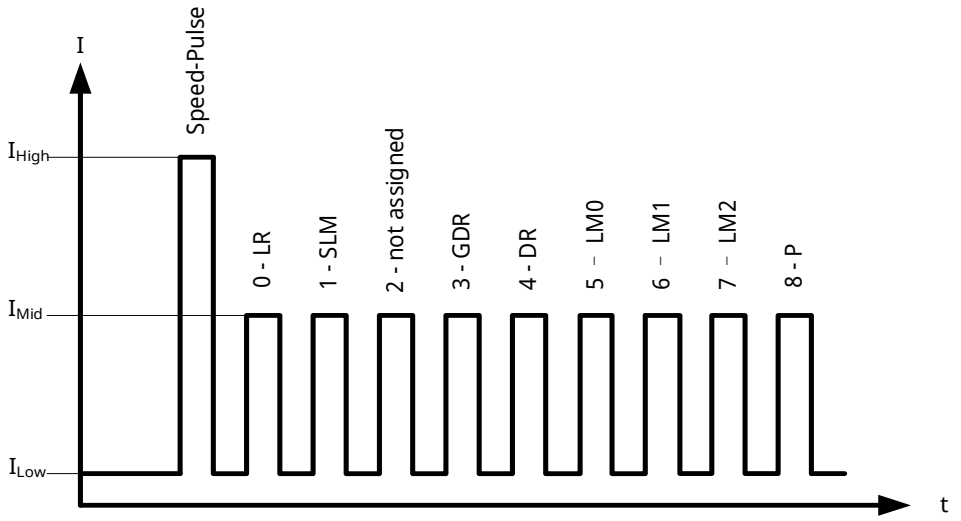


Fig.4 ZAK data bit encoding

10.1.1 Data Bits

Bit	Description	Symbol	Value	Explanation
0	Error bit, Airgap reserve	LR	0	“1” , if $\triangle B < \triangle B_{LR}$, (1 = error)
1	Validity of signal amplitude measurement	SLM	1	0 = measurement of LM0, LM1, LM2 is valid; 1 = invalid
2	not assigned		0	
3	Direction validity	GDR	0	“1” = valid, “0” = invalids
4	Direction of rotating information	DR	0	“0” = direction positive
5	Air gap gauge	LM0	0	LSB of airgap gauge
6		LM1	0	
7		LM2	0	MSB of airgap gauge
8	Parity	P	Calculating result	Always set to get even parity (inclusive Parity bit itself)

10.1.2 Manchester Encoding

The data protocol is Manchester-coded. This means the value of a bit is coded in a rising or a falling of the signal between the middle-current value (I_{mid}) and low-current (I_{low}) in a certain time window. A transition from low to middle corresponds to "1", a transition from middle to low corresponds to "0". Falling and rising edge of sensor output current starts in the middle of data protocol (=tp/2), see the bottom of the example in Figure 5.

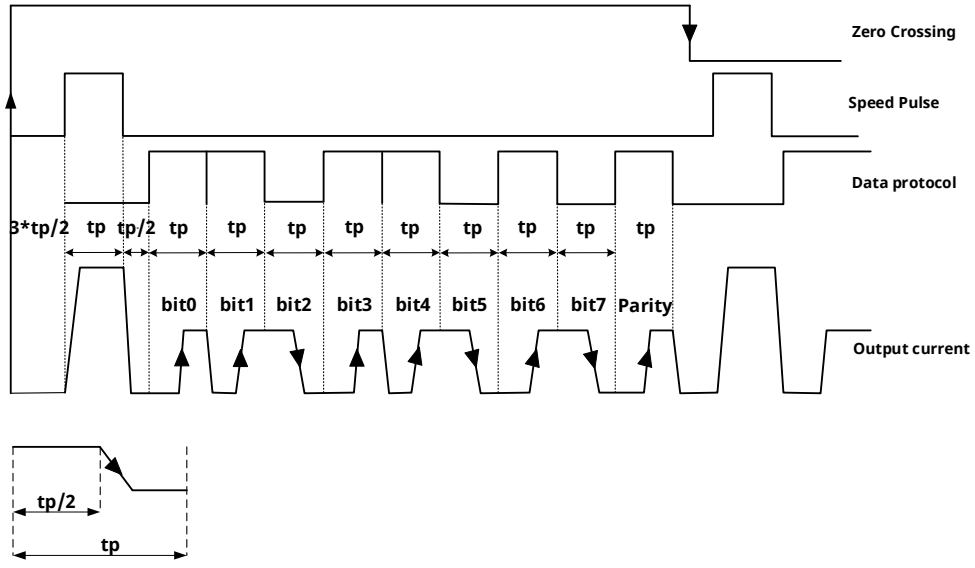


Fig.5 Manchester Encoding

10.1.3 AK Protocol At Normal Speed

At normal speed (signal frequencies less than 1800Hz) all data bits are transmitted. At the beginning the initial bit (I_{low}) is sent for tp/2. Then the speed pulse with duration tp is issued which is followed by a current level Ilow for tp/2. After that the data protocol is sent.

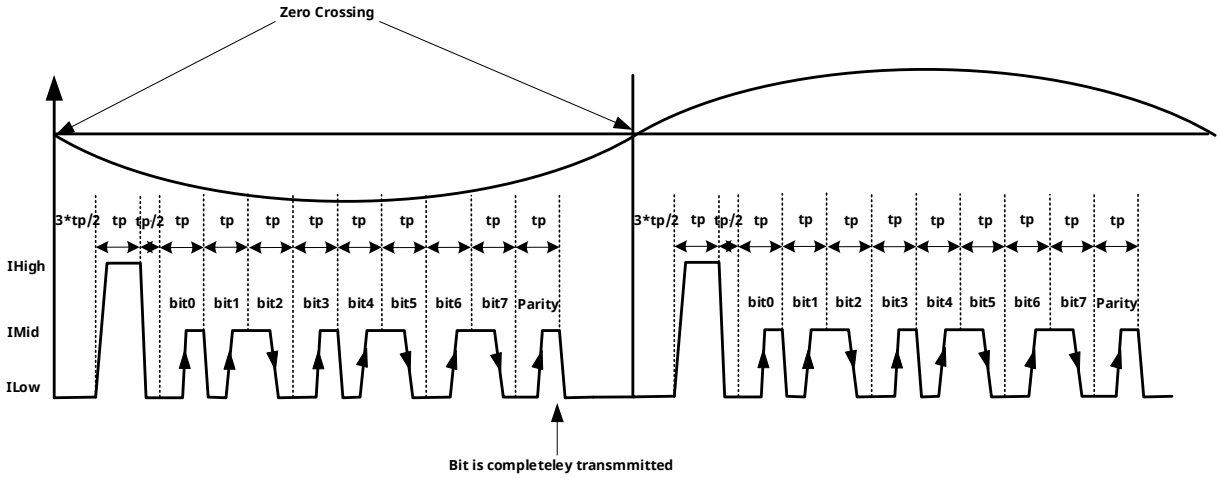


Fig.6 AK Protocol at normal speed

10.1.4 AK Protocol At High Speed

The higher the speed, the shorter the data protocol (the last bit is cut off). The following table shows the number of transmission bits at different signal frequencies. At high speeds, the serial data protocol shortens because the time to the next speed pulse is shorter than the protocol period. Therefore, the last data bit is "cut off". Within each speed range, the number of additional information bits transmitted should be as many as possible. Called bit damaged parts of the transmission bit output are suppressed. The shortening of the protocol will not result in any "bit defect" (bits that have not been fully transmitted). This means that the bits affected by the shortening will be transmitted completely in any case, that is to say, the bits that have already started to be transmitted must also be transmitted to the destination. The current level I_{low} must be output instead of the bits affected by shortening. Bit defect can be reliably suppressed across all speed ranges of the sensor and in all normal operating states, that is, in the static protocol.

Electric Signal frequency	Typical Number of data bits transmitted
＜1818Hz (1800Hz)	9(bit 0 - bit 8)
＜2000Hz (2000Hz)	8(bit 0 - bit 7)
＜2222Hz (2200Hz)	7(bit 0 - bit 6)
＜2500Hz (2400Hz)	6(bit 0 - bit 5)
＜2857Hz (2800Hz)	5(bit 0 - bit 4)
＜3333Hz (3200Hz)	4(bit 0 - bit 3)
＜4000Hz (4000Hz)	3(bit 0 - bit 2)
＜5000Hz (5000Hz)	2(bit 0 - bit 1)

10.1.5 Data Protocol for Standstill

If for a longer time than t_{stop} no increment is recognized, the IC starts to send the standstill-protocol. This protocols is sent every 150ms +/- 20%. In this protocol the current value of the speed-pulse is set to I_{mid} and all the other bits are transmitted like described before. For very slow wheel speeds more than one standstill protocol can be issued between consecutive speed pulses.

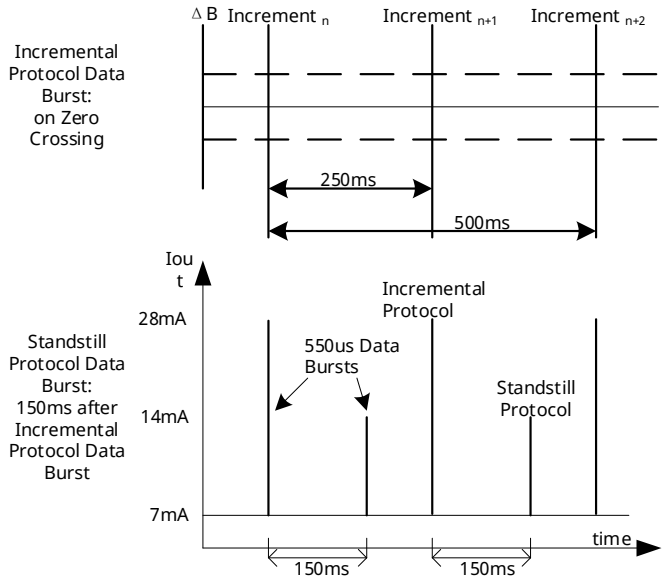


Fig.7 Standstill protocol

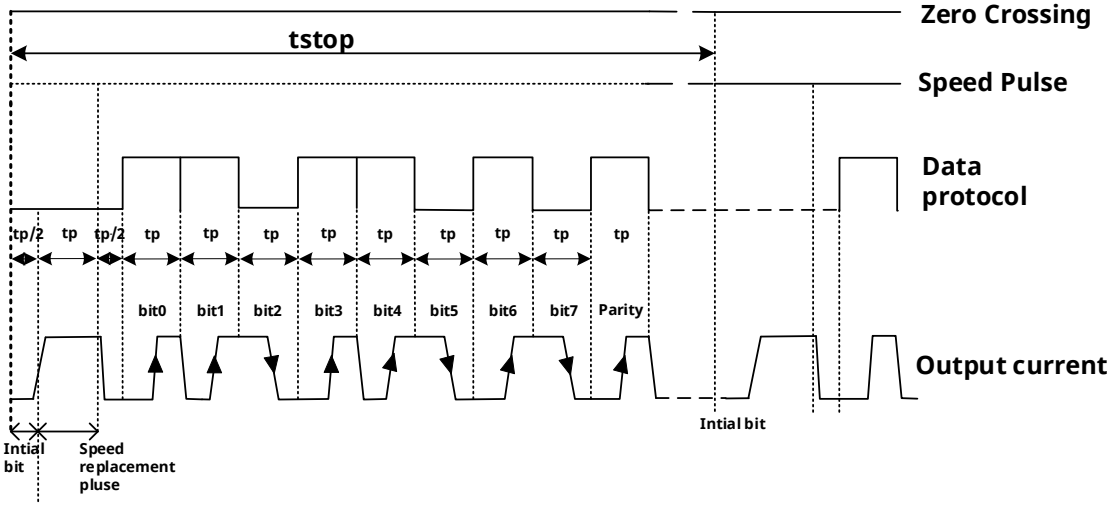


Fig.8 The output situation of the protocol in a static state

Bit transfer description in a stationary state:

If an increment of the input magnetic signal is detected, the static protocol will be terminated. The speed pulse I_{high} has priority with the start bit (level I_{low}). Because the static protocol also needs to suppress "bit defect", the interruption of the protocol can actually only occur between two data bits and cannot occur during the ongoing bit transmission process. The initial bit ensures that there is always a current level I_{low} before the velocity pulse, lasting for at least $t_p/2$. This helps the ECU (Electronic Control Unit) detect speed pulses.

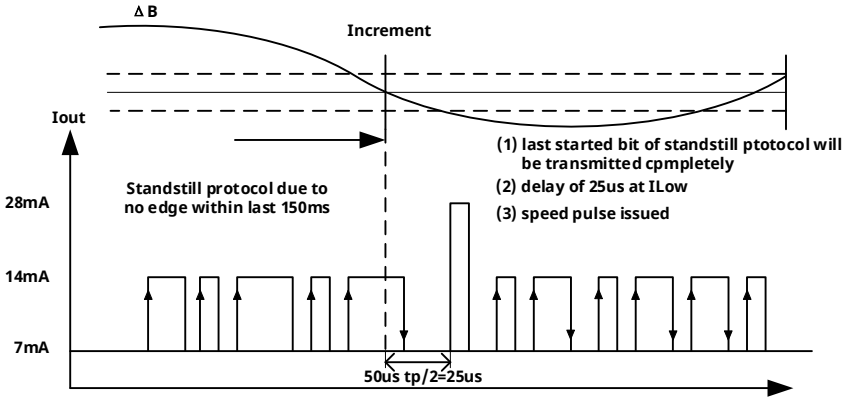


Fig.9 Starting wheel movement during standstill protocol using bit stump suppression

Handling of "Direction Validity" and "Direction" at the standstill protocol:

At any standstill DR is transmitted as zero (default value) and GDR is transmitted as invalid (=0). With the first 5 standstill protocols in a row, the direction algorithm is reset. Therefore at following next three zero crossings (speed pulses) direction detection and change of direction detection takes place (GDR=invalid, DR=default) and GDR is valid and corresponding direction is output at third speed pulse after standstill.

Handling of "Validity of signal amplitude measurement" within standstill protocol:

Validity (SLM) of signal measurement is transmitted as 1 (invalid) and signal amplitude (Level in relation to LR) is transmitted as 0 during standstill protocol. With the first 5 standstill protocols in a row, the SLM/LM is reset to invalid. SLM remains invalid until two new extrema in dB are found. Depending on the amplitude of dB and phase of the standstill protocol, SLM is valid with the second, third or fourth speed protocol after every 5th standstill protocol.

Handling of Error Bit "Air Gap Reserve" (=LR bit) within standstill protocol:

It is transmitted as "0" (no error) in the standstill protocol. It is reset to 0 with the first 5 standstill protocols in a row. The standstill protocol LR remains "0" (no error) until two new extrema in dB are found. The initial bit enables the speed pulse to always be preceded by a current level I_{low} for a duration of at least $t_p/2$. This is helpful for the detection of the speed pulse in the ECU.

10.1.6 Bit Defect Suppression

This section will introduce the implementation method of bit defect suppression for wheel speed sensors (WSS). The principle of achieving bit defect suppression is as follows:

Constant time shift of velocity pulses and data protocol outputs:

At the start of a new protocol, the sensor output is always completely offset by one bit time t_p. This is equivalent to a time output offset, and the effect is as follows:

The initial bit does not start immediately at the beginning of a new protocol, which may occur during highspeed data protocols. Instead, t_p always initially waits for a time offset within which it monitors the output of the last ongoing protocol. If the bit output is still active, it will be fully transmitted without being cut off. This will

effectively prevent bit interruption. During this offset time t_p, the next possible data bit of the last protocol will be suppressed. In this way, the transfer of the current bit will be completed, while the transfer of the other bits (of the last protocol) will be blocked. Start transmitting the initial bit at the end of the offset time. The advantage of this program: It is also effective in stationary protocols. If new increments of the input magnetic signal are detected during a stationary protocol in progress, the current bit transfer does not end in any "bit defect". The transmission of additional bits will be suppressed. After the delay phase ends, new transmissions begin with the initial bit $t_p/2$, followed by the speed pulse and the data protocol.

The following figure shows the effect of suppressing bit defect in three representative cases based on the above method.

Case 1: Not cutting off the previous protocol.

There is enough time between two consecutive protocols to transfer all the bits. However, the new protocol begins at the moment when a new increment of the input magnetic signal is added, and its perpetual output offset length is t_p . Then comes the initial bit width $t_p/2$, followed by velocity pulses, etc.

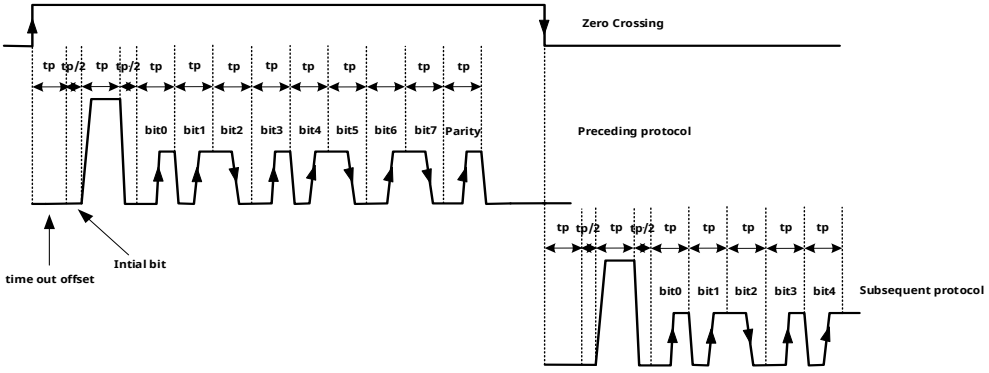


Fig.10 Does not cut off the previous protocol

Case 2: The last bit of the previous protocol is cut off.

When the last bit of the current protocol is still being transmitted, if there is a new increment in the magnetic input signal, the time between the two consecutive protocols is no longer sufficient. At this point, the new protocol starts anew with a constant output offset of tp . However, the sensor is now aware that bit transmission is still going on. This will complete the transfer in the current running output offset. After the output offset ends, the initial bits are transmitted starting at tp/2, followed by velocity pulses, etc.

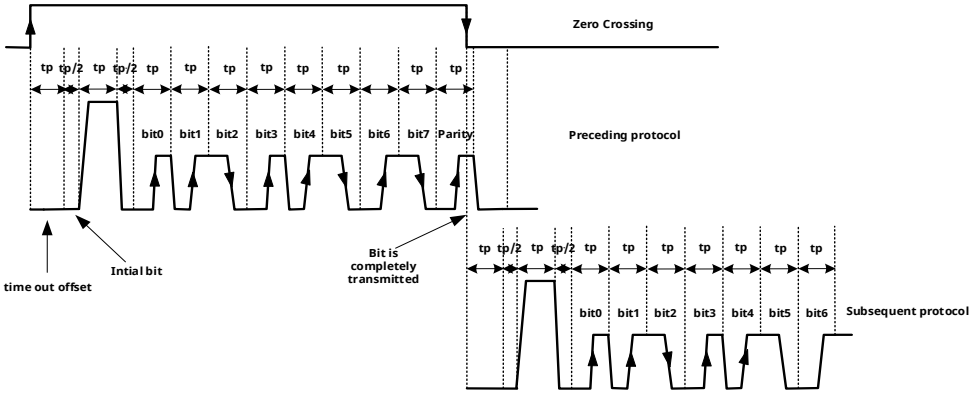


Fig.11 The last bit of the previous protocol is cut off

Case 3: A few bits of the previous protocol are cut off.

For example, when there is a new increment in the input signal while the 6th bit of the previous protocol is still being transmitted. At this point, the new protocol starts again with a constant-time output offset of length t_p . The sensor will be aware that the transmission is still going on. During the current running output offset time, bit 6 of the previous protocol will be fully transmitted. In addition, the still missing bits 7 and 8 (parity) are suppressed and no longer transmitted. As a result, the line is restored to clean again after the output offset ends, the initial bit is transmitted after $t_p/2$, followed by the velocity pulse, etc.

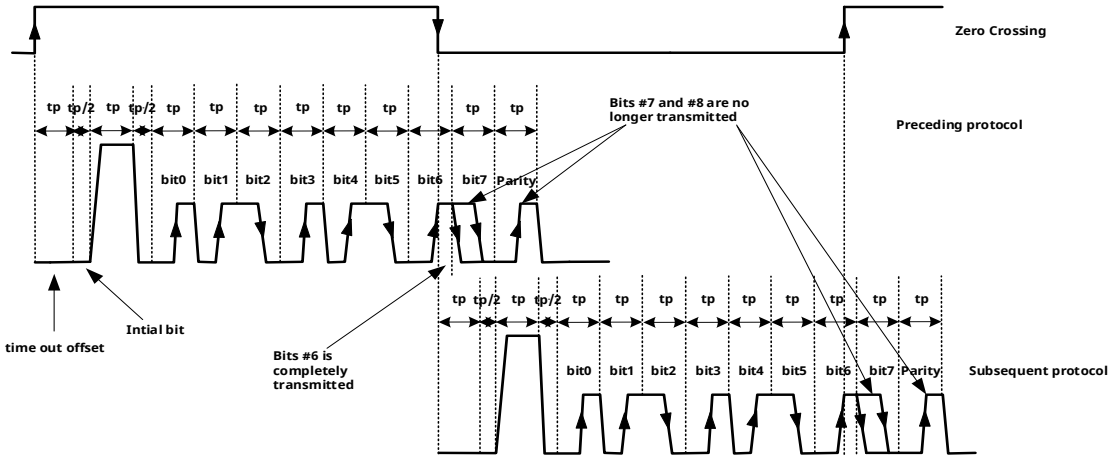


Fig.12 A few bits of the previous protocol are cut of

10.2 PWM Protocol description

Stand Still mode: When the installation distance is far or the gear does not rotate, △B is less than 7GS, the chip outputs a waveform with a pulse width of 1.44ms.

Alarm mode: When the installation distance is at the critical position and △B is between 7GS and 12GS, the chip outputs a waveform with a pulse width of 45μs.

EL mode: When the installation distance is moderate, △B is between 12GS and 65GS, the rotational speed is slower, the pulse frequency is less than 117Hz, and the forward rotation (VDD→GND) outputs a 360μS pulse width waveform in DR-L&EL mode Reverse (GND→VDD) output 720μS pulse width waveform in DR-R&EL mode; At higher rotational speeds with a pulse frequency greater than 117Hz, forward rotation (VDD→GND) outputs a 90μS pulse width waveform, and reverse rotation (GND→VDD) outputs a 180μs pulse width waveform.

DR Mode: When the installation distance is close, △B is greater than 65GS, regardless of speed, forward rotation (VDD→GND) outputs a 90μs pulse width waveform, mode is DR-L, reverse (GND→VDD) output a 180μs pulse width waveform in DR-R mode.

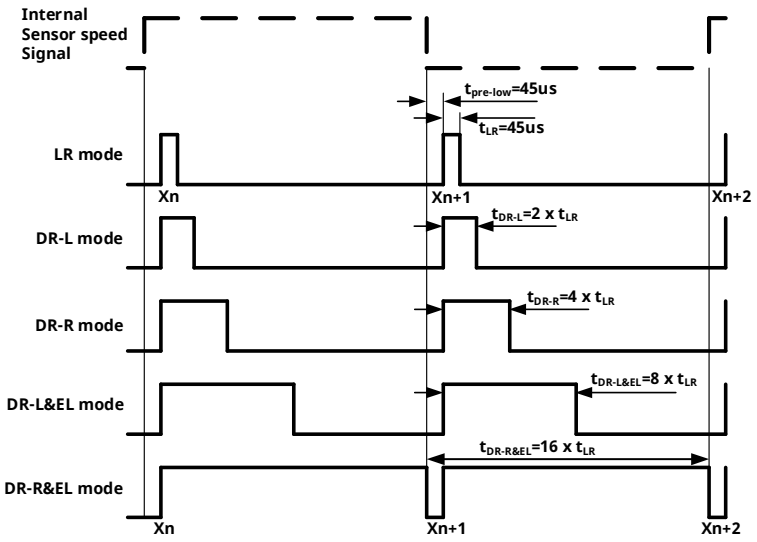


Fig.13 PWM timing definition

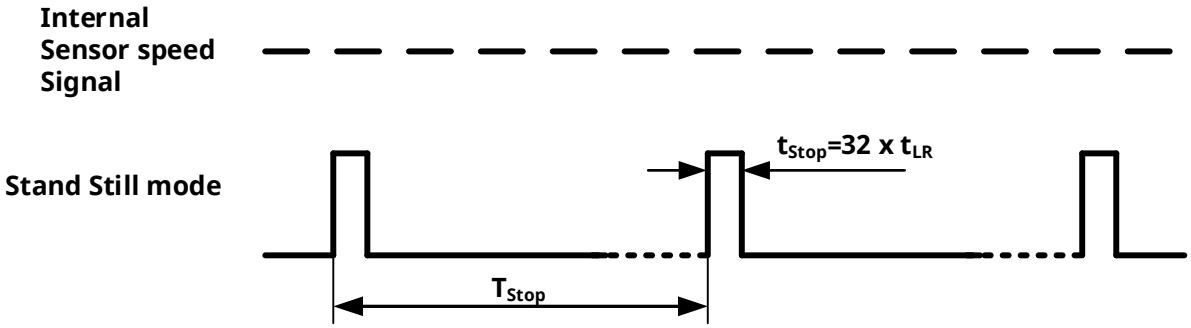


Fig.14 Stand Still mode timing definition

10.3 Uncalibrated and Calibrated Mode

After an initial calibration delay time t_{d_input}, the differential magnetic signal dB is tracked by an analog to digital converter (ADC) and monitored within the digital circuit. For detection the signal needs to exceed the internal threshold DNC (digital noise constant). When the signal slope is identified as a falling (or rising) edge and the signal change exceeds the DNC, the first extrema is located and first output pulse is triggered. The digital noise constant value is changed accordingly to magnetic field amplitude, leading to a change in phase shift between magnetic input signal and output signal. This value of the digital noise constant is determined by the signal amplitude. First DNC (=2 x dB_{limit}), indicated as arrows in figure below. A second output is triggered when the signal change exceeds again the value of the new DNC (calculated by (min1 + max 1)/2) in the following rising (respectively falling) edge. When a maximum and minimum was found an offset correction will take place. This leads to a phase shift of output signal and the sensor enters the calibrated mode. In calibrated mode switching is triggered by the zero crossing of the differential magnetic signal. The min/max detection is reduced to 1/4 of peak-peak. In calibrated mode minimal DNC is 2 x dB_{limit}. Out of this consecutive speed pulses have a nominal delay of about 180°.

Handling of additional information bits in uncalibrated and calibrated mode:

Signal amplitude measurement: SLM is valid if two valid extrema are found (the first extrema after power on is

invalid). Latest with fourth protocol SLM is valid.

Startup at high frequencies could lead to shortened protocol. The bit suppression according Chapter “Bit Stump Suppression” is executed.

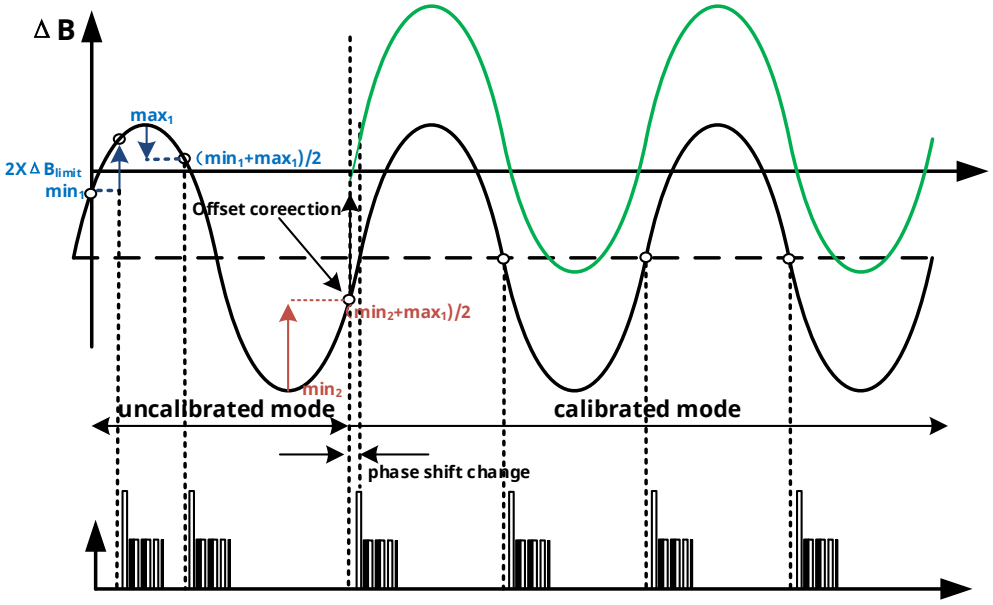


Fig.15 Example for startup behavior and change form uncalibrated into calibrated mode

10.4 Hysteresis definition

Adaptive hysteresis has the advantage of large hysteresis in small small gaps (large signals). Compared with fixed hysteresis, tiny vibrations do not cause additional switching. According to Figure 17, the calculation formula for adaptive hysteresis is 25% of the difference between the peak-to-peak velocity signals. The minimum hysteresis is derived from the fine-tuning setting.

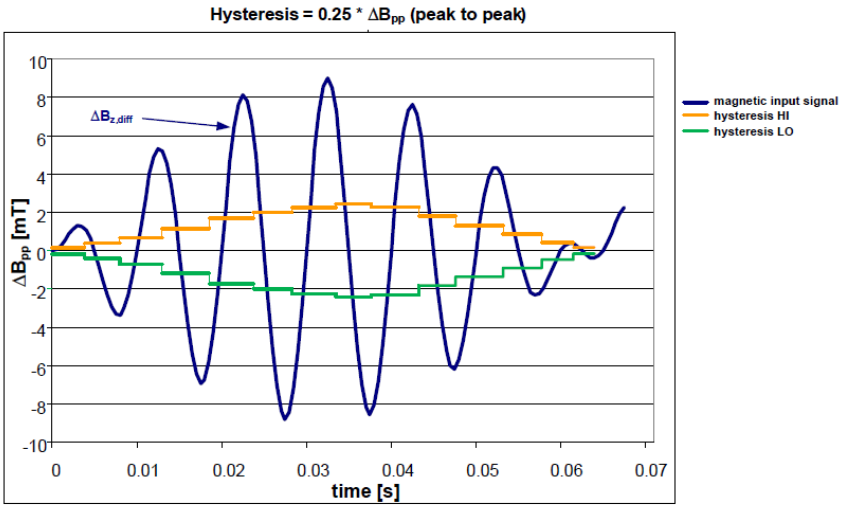


Fig.16 Adaptive Hysteresis

10.5 Direction changes, vibrations, and abnormal states

During normal operation, SC9683 and SC9684 are subject to abnormal events such as changes in the direction of target rotation, target vibration, and sudden changes in the air gap. During calibration, output pulses with direction information are immediately transmitted to the output terminal. Depending on the target design, air gap, and target phase, there may be momentary errors in direction. After changing direction in running mode, the direction change is immediately transmitted to the output.

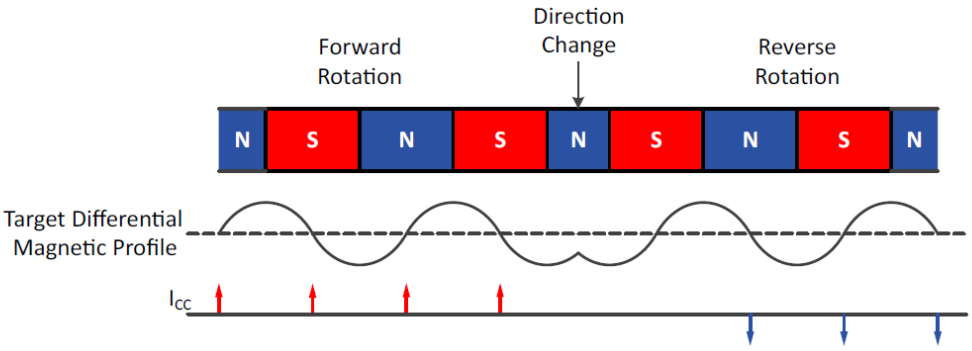


Fig.17 Direction change

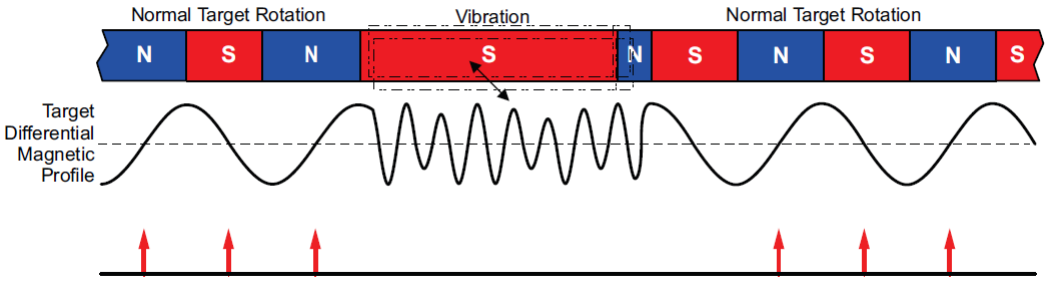


Fig.18 Vibration behavior

11. EMC(Electromagnetic Compatibility)

11.1 EMC circuits

The EMC test circuit with reverse bias and overvoltage protection is shown below.

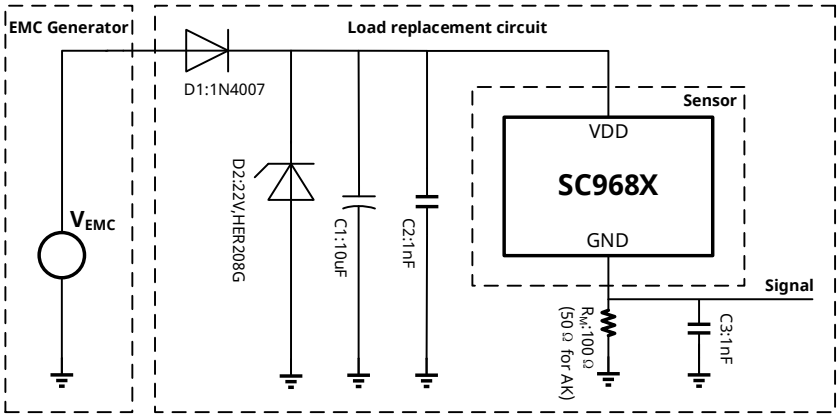


Fig.19 EMC test circuit

11.2 ISO 7637

Refer to ISO 7637-2; 2004; ΔB=2mT (sinusoidal signal amplitude); V_{DD}=13.5V; f_B =100Hz, T_A=25°C, R_M=30Ω

Symbols	Parameters	Level/Type	Grade
$V_{MEC\_7637\_2}$	Test Pulse 1	IV /-100V	C
	Test Pulse 2a	IV /75V	A
	Test Pulse 2b	- /10V	C
	Test Pulse 3a	IV /-150V	A
	Test Pulse 3b	IV /100V	A
	Test Pulse 4	IV /-7V	B
	Test Pulse 5a	IV /86.5V	C
	Test Pulse 5b	Us=28.5V	C

Refer to ISO 7637-3 1995; ΔB=2mT (sinusoidal signal amplitude); V_{DD}=13.5V; f_B =100Hz, T_A=25°C, R_M=30Ω

Symbols	Parameters	Level/Type	Grade
$V_{MEC\_7637\_3}$	Test Pulse 1	IV /-30V	A
	Test Pulse 2	IV /30V	A
	Test Pulse 3a	IV /-60V	A
	Test Pulse 3b	IV /40V	A

11.3 ISO 11452

Refer to ISO 11452-3 2001; ΔB=20Gs, V_{DD}=13.5V; f_B =100Hz, T_A=25°C

Symbols	Parameters	Level/Type	Grade
$E_{TemCell}$	TEM test	IV/250V/m	CW；AM=80%，f=1kHz

Refer to ISO 11452-4 2011; Stress =1-400MHz; V_{DD}=13.5V; f_B =100Hz, T_A=25°C

Symbols	Parameters	Level/Type	Grade
BCI open		200mA	I
BCI close		200mA	I

Refer to ISO 11452-8 2007; V_{DD}=13.5V; f_B =100Hz, T_A=25°C

Symbols	Parameters	Level/Type	Grade
ITMF_DC		2mT	I
ITMF_AC			II

12. Typical application circuit

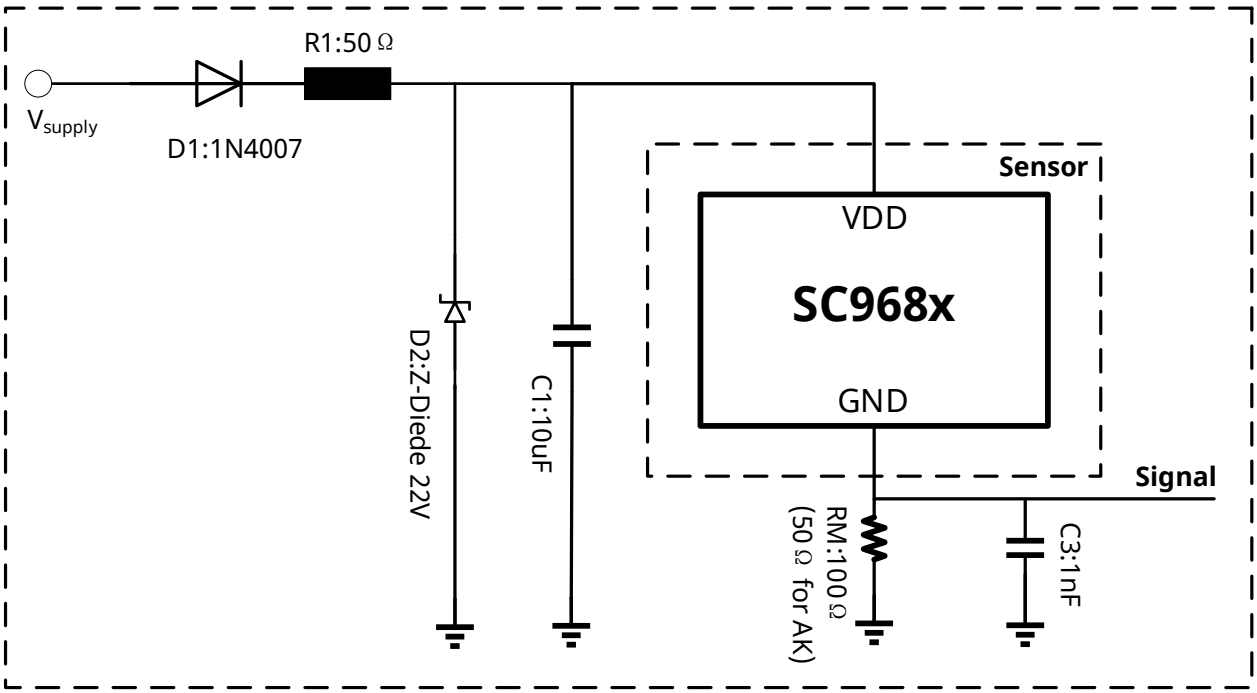
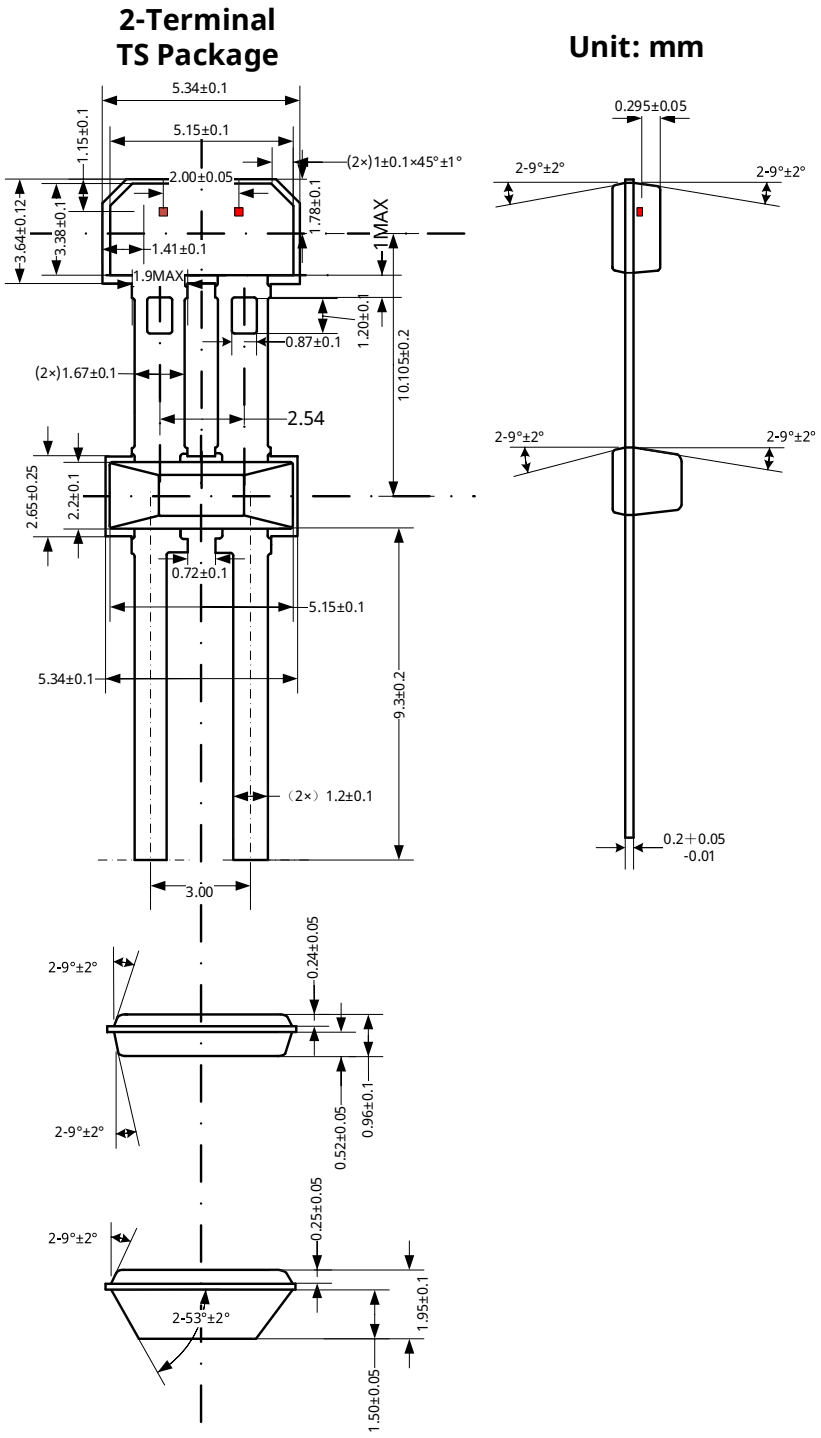


Fig.20 Typical application circuit

13. Package information TS-2



Notes:

1.Exact body and lead configuration at vendor's option within limits shown.

2.Height does not include mold gate flash.

3.The spacing between two hall plates is 2.0mm.

Where no tolerance is specified, dimension is nominal.

Fig.21 TS-2 Package information

14. Tape information TS-2

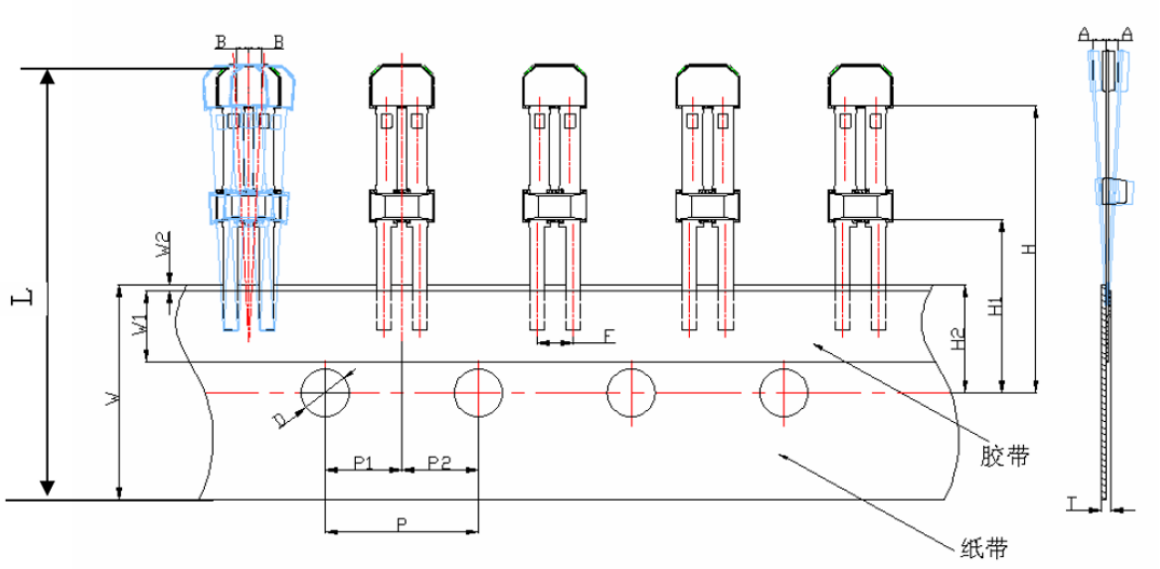
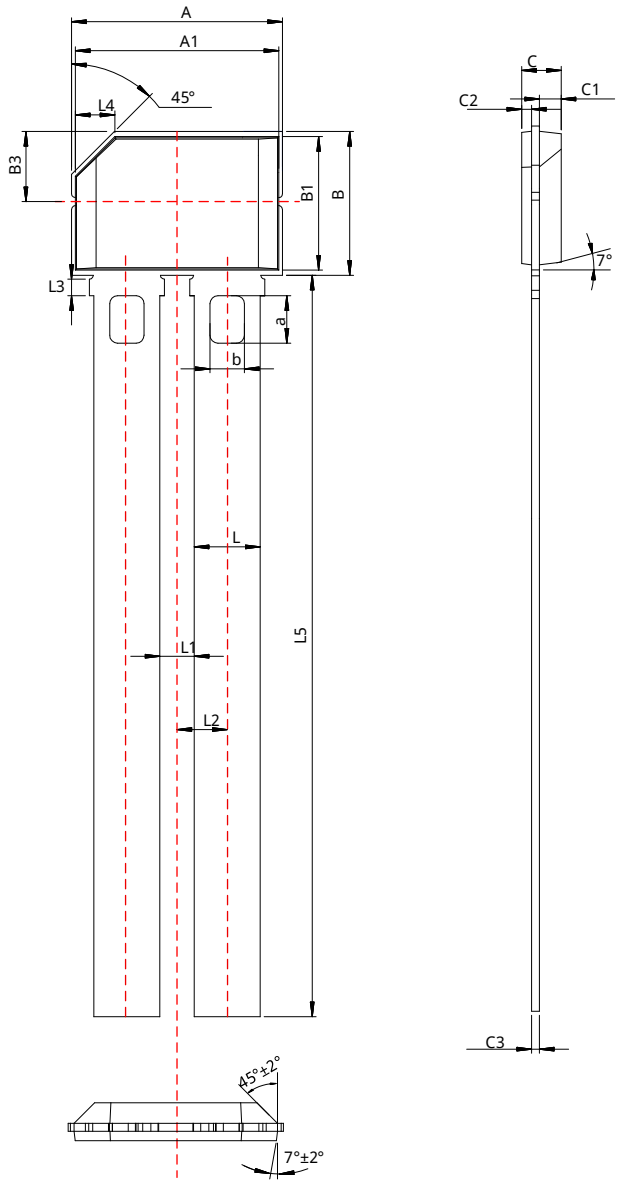


Fig.22 TS-2 Tape dimensions

Symbol	Specification (millimeters)
A	0±0.5
B	0±0.3
D	4±0.3
F	3±0.2
H	24±0.5
H1	14.48±0.5
H2	9±0.5
L	36.4±0.2
P	12.7±0.3
P1	6.35±0.4
P2	6.35±0.4
T	≤1
W	18.0±0.3
W1	6±0.5
W2	0-0.8

15. Package information TS-2A

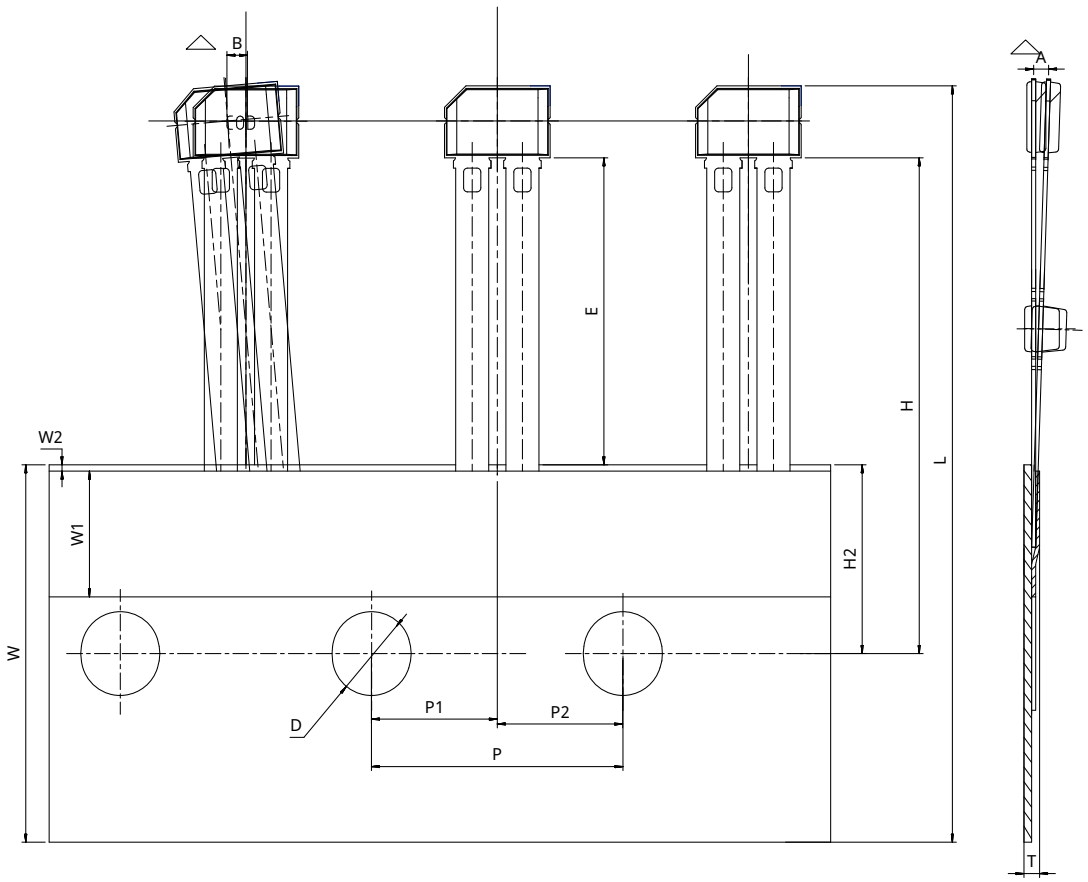
TS-2A Package Outline



Dimensions in Millimeters			
Symbol	Min.	Typ.	Max.
A	5.24	5.34	5.44
A1	5.05	5.15	5.25
B	3.52	3.64	3.76
B1	3.28	3.38	3.48
B2	1.68	1.78	1.88
C	0.92	0.96	1.00
C1	0.47	0.52	0.57
C2	0.19	0.24	0.29
C3	—	0.20	—
L	1.62	1.67	1.72
L1	0.82	0.87	0.92
L2	—	1.27	—
L3	—	0.37	—
L4	—	1.00	—
L5	18.72	18.77	18.82
a	1.15	1.20	1.25
b	0.82	0.870	0.92

Fig.23 TS-2A Package information

16. Tape information TS-2A



TS-2A tape dimensions			
Symbol	Spec（mm）		
△A	0±0.5	P	12.7±0.3
△B	0±0.3	P1.P2	6.35±0.4
D	4.0±0.3	T	1 max
E	15.05±0.25	W	18.0±0.3
H	24±0.5	W1	6.0±0.5
H2	9.0±0.5	W2	0-0.8
L	36.4±0.2	/	/

Fig.24 TS-2A Tape dimensions

17. Revision History

Revision	Date	Description
Rev. E0.1	2022-04-27	First edition specification sheet
Rev. E0.2	2023-12-12	Increase jitter suppression
Rev. A1.0	2025-03-26	Unified datasheet format

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